CARL VON OSSIETZKY universität OLDENBURG

DLR Deutsches Zentrum für Luft- und Raumfahrt

Institut für Vernetzte Energiesysteme

Real-Time Hybrid Simulation and Power Hardware-in-the-Loop Characterization of Distribution Grid Models

Master Thesis

By

Moiz

Matriculation Number: 4704237

Postgraduate Program Renewable Energy (PPRE)

Institute of Physics

First Examiner:	Prof. Dr. Carsten Agert
Second Examiner:	Dr. Stefan Geißendörfer
Technical Supervisor:	Holger Behrends

Postgraduate Programme Renewable Energy PPRE

Oldenburg, Germany, 18th September 2020.

This Master thesis is submitted in partial fulfillment of the requirements for the degree of Master of Science (MSc) in Renewable Energy at the
Carl von Ossietzky University of Oldenburg.

ABSTRACT

The grid codes implemented by several countries demands distributed generators to provide voltage support through provision of reactive power by inverters. With increasing inverter-based generation it is essential to test local autonomous control of inverters in a controlled environment to investigate grid stability. Real-time power hardware-in-the-loop (PHIL) concept is an efficient tool for such evaluations. This thesis focuses on the development of a PHIL setup to examine the issues linked with the power interface and also the hardware under test when it is controlled virtually to inject/draw desired powers into/from the simulated grid.

In the first phase, a simulation testbed is developed which includes distribution grid models following the topology from MONA projects. The models are developed completely in the phasor domain which enables to perform dynamic power flow and voltage stability analysis. The feed-in unit and the load are integrated with actual power profiles. It is a hybrid load modelled as a grid following inverter injecting synchronized currents into the grid based on power sink or feed-in. For reactive power management during the feed-in, smart inverter control functions are developed. Different reactive power control strategies are tested and its impact on the grid voltage is observed. For validation of the grid model and reactive power management functions, the results of some scenarios are compared from two different power distribution system analysis platforms.

In the second phase, a hybrid simulation (Phasor – EMT) model is developed. The aim is to have an interface to facilitate the handling of discrete waveforms during PHIL simulation. The equivalent circuits (Norton and Thevenin) are used to represent one sub-system in another and to ensure proper transfer of variables over the interface bus where the network partition is performed. The scenarios implemented to observe the operation of the developed hybrid simulation model show that the parameters (voltage and current) at the interface bus from both the domains are transformed accurately. Further, the uni-directional and bi-directional power exchange is also analyzed at the interface bus.

Finally, in the last phase, the PHIL simulation is executed with MONA-8002 distribution grid simulated in real-time. Proposed unconventional PHIL setup involves two physical hardware components; a power interface (voltage-controlled amplifier) serving as grid-simulator and other as hardware under test (current-controlled amplifier) controlled from the simulation platform. The mathematical model is executed on multi-core processors of real-time simulator with a sample time of 100 µs. Going lower than this causes the processors to overload. Different configurations of hardware under test at the point of common coupling are tested with the virtual simulated grid. The results show that the hardware in amplifier mode injects reactive power into the virtual grid depending upon the voltage level due to its parasitic capacitance. At nominal standard voltage, a capacitive reactive power of roughly 1.3 kvar is present. Further at low power demands, the current waveform gets very distorted due to the increased harmonic content. To alleviate the effects of parasitic capacitance two compensation methods are introduced and tested. After implementing the compensation, the average default reactive power from the hardware under test i.e. current-controlled amplifier is reduced.

ACKNOWLEDGEMENT

I would like to express my deepest gratitude to my group leader Dr. Stefan Geißendörfer and project leader Mr. Holger Behrends at the DLR – Institute for Networked Energy Systems for their constant support and guidance. They always enabled me to work conveniently alongside with my studies and made it possible for me to work with the cutting-edge laboratory power equipment's for this thesis project. My working group and the institute have played a vital role in my studies, strengthening my research abilities by working on research projects including this one. Being from an electrical engineering background with my master's degree specialization focused on grid systems integration, it was the perfect opportunity for me to gain practical skills in a research-oriented group of power system technologies.

Secondly, I would sincerely like to thank the German Academic Exchange Service (DAAD) for providing me the scholarship to pursue my Master studies. This would not have been possible without the financial support from DAAD through Development Related Post-Graduate Course scholarship.

Finally, the credit goes to my parents for believing in me and giving me the moral support to pass through this two-years exciting journey in Germany.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

ABBREVIATIONS

CC amplifier: Current-Controlled Amplifier

Cosφ: Power Factor

DER: Distributed Energy Resources

DG: Distributed Generators

DSO: Distribution System Operators

DUT: *Device Under Test*

EMT: Electromagnetic Transient

FPGA: *Field-programmable gate array*

HUT: *Hardware under Test*

ITM: *Ideal Transformer Model*

LV: Low Voltage

LVDG: Low Voltage Distribution Grids

PA: *Power Amplifier*

PCC: Point of Common Coupling

pf: Power Factor

PHIL: Power Hardware-in-the-Loop

PI: *Power Interface*

PID Controller: *Proportional Integral Derivative Controller*

PV: Photovoltaic

Q-Control: Reactive Power Control

Q-Management: *Reactive Power Management*

RT: Real-Time

RTS: *Real-Time Simulator*

TS: Transient Stability

1 Introduction

The past few years have experienced an unprecedented growth of distributed energy resources (DER) globally. Among these, the most dominant renewable resources being exploited are hydro, wind and solar (via photovoltaic systems). Germany, among other countries, is also active in this energy transformation which is known natively as 'Energiewende'. It is setting optimistic goals to achieve considerable share of electricity from renewables by 2050. In Germany, the concentration of photovoltaic (PV) systems alone has experienced an exponential increase in recent years. From this cumulative installed PV capacity, most of the expansion is experienced in low voltage distribution grids (LVDG), amounting to a total of 22GW until 2015 [1]. The following graph in **Figure 1.1** shows the share of renewable energy in gross electricity consumption and increasing share of PV (yellow bars) along the years.

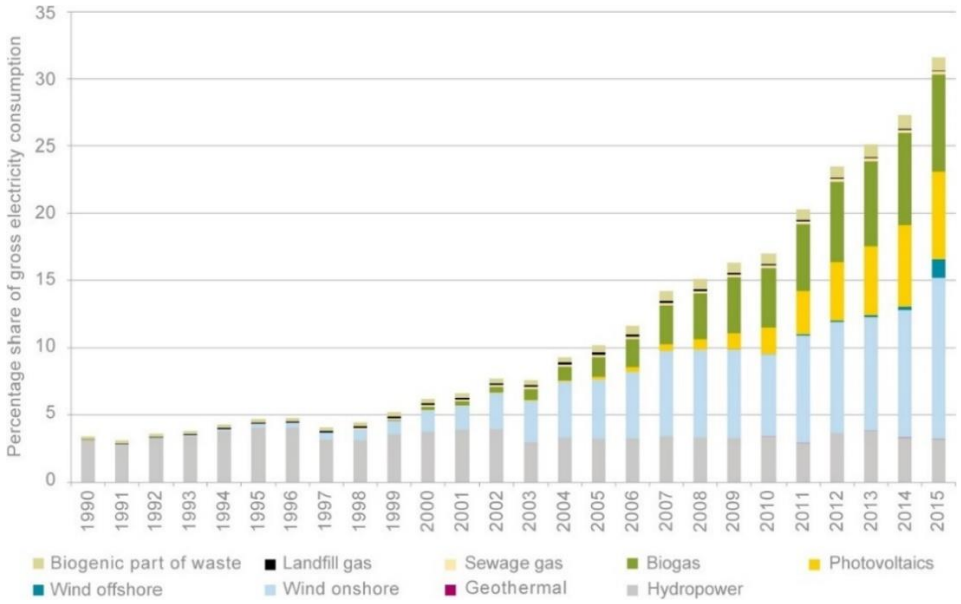


Figure 1.1 Increasing share of PV in gross electricity consumption in Germany [2].

To streamline PV integration practices, the renewable energy act, 'Erneuerbare Energien Gesetz (EEG 2017) [3]' provides the requirements regarding grid integration of DER. Further, grid integration directives VDE-AR-N 4105 [4] also highlights the practices for PV systems feeding into the low LVDG and calls for voltage regulation support through provision of reactive power. Unlike conventional generators, the power produced by PV systems is interfaced into the electrical grid via power inverters. This addition of distributed generators (DG) poses underlying technical challenges for network operators such as voltage regulation and voltage unbalance.

The inverter's capability to provide/consume reactive power can help to compensate for reactive power balance in the grid, provide voltage stability at the point of common coupling and enlarge the hosting capacity of DER. Various simulation studies of smart reactive power management (Q-management) via autonomous control has shown that the inverters react promptly towards system changes but its application in real-time operation with conventional power grids is a concern for distribution system operators and needs to be tested in a controlled environment. Power Hardware-in-the-Loop (PHIL) simulation technology has provided an efficient platform to perform such laboratory experiments integrating real hardware and controls, to study the stability of the power

systems. The **Figure 1.2** below illustrates that the voltage level exceeds at the point of common coupling due to the active power feed-in and reactive power controls the voltage rise.

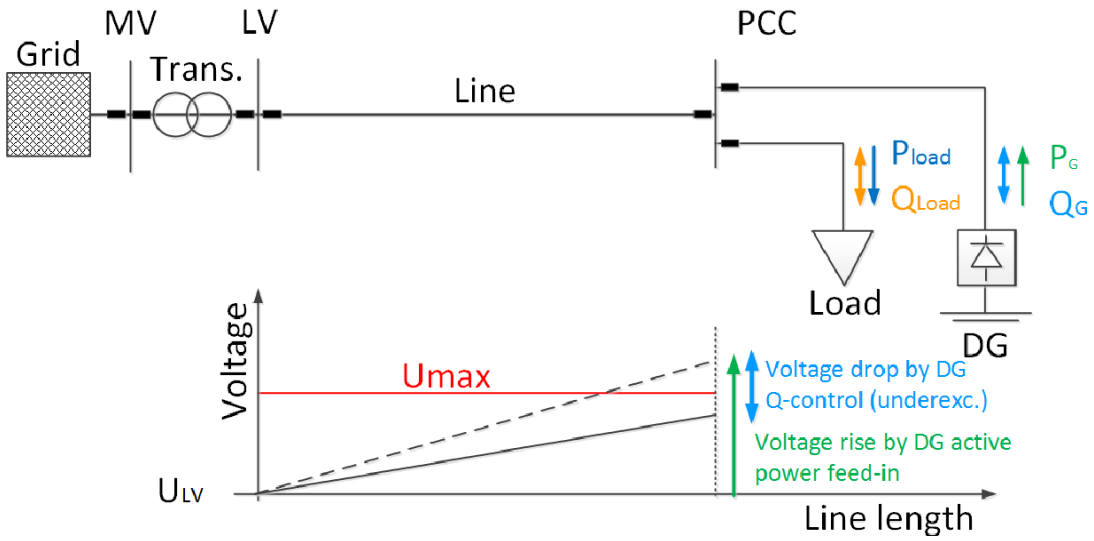


Figure 1.2 Reactive power support to limit the voltage rise at feed-in point [5].

In this thesis, two different low voltage distribution grid networks are developed in complete phasor framework in Simulink-MATLAB® [6]. The load and the feed-in unit are modelled as a simple P-Q source depicting a grid following inverter. To represent the loads, actual household profiles [7] are integrated at the buses, similarly for feed-in units actual PV power profiles [8] are used. The Q-management functions are implemented as a top layer for the inverter with state-of-the-art control strategies including voltage dependent reactive power injection. A detailed power flow analysis is performed in phasor domain, with and without feed-in units integrated into the distribution grid. The inverter model developed serves the purpose of analyzing the impacts of reverse power flow on the grid voltage levels. Additionally, the response of different Q-management functions is analyzed, and it is observed that it supports voltage regulation at the point of common coupling.

For the PHIL setup, executing the complete grid model in discrete domain with a sample-time in the range of micro-seconds would overburden the real-time simulator processors and is not viable. Therefore, in this thesis, a hybrid simulation model is developed in Simulink-MATLAB modelling only part of the grid in discrete domain whereas the majority of the grid is modelled in phasor domain. The segregation is performed at the interface bus at which the hardware will be connected in the PHIL setup. The Thevenin and Norton equivalent circuits are used to represent one sub-system in another respectively, an idea adopted from the PhD dissertation [9]. The equivalent voltage and current sources are updated dynamically during the hybrid simulation. The results show that the interface between the two sub-systems works in synchronization with accurate exchange of powers at the interface bus.

In the scope of PHIL test, the voltage type interface model is adopted as the interface topology. The Speedgoat real-time target machine holds the mathematical model of MONA-8002 grid executed in real-time. The setup involves a voltage-controlled switched-mode power amplifier as a power interface (PI) to emulate the voltage of the interface bus from the virtual grid model. A minute phase delay and offset are observed between the emulated and the amplified output voltage. The current

through the hardware under test (HUT) is measured and fed back to the virtual simulated grid through a controlled-current source. Different configurations of the HUT are tested, as a constant load bank, as an amplifier in RLC load simulation mode and as a current-controlled (CC) amplifier. The parasitic capacitance effect of the HUT's operation in CC amplifier mode is discussed in detail. To mitigate the illusionary reactive power, compensation methods are developed by incorporating a delay in the reference current signal in time domain. Further, at low active power demands the HUT introduces significant harmonics in the system which affects the measurements and stability of the PHIL setup. For the real-time simulator (RTS), it is observed that the sample time of less than 100 µs are not possible due to the computational limitation of the processors. The results from the PHIL simulations discusses the limitations to test the Q-management on the HUT and to operate it resembling as a prosumer with integrated load and PV profiles.

The motivation behind this study is firstly, that not much literature is found in the context of smart grid PHIL simulation with a complete Simulink-MATLAB interface and Speedgoat target system as RTS. Secondly for integration studies, usually the HUT in PHIL simulation is a commercial device for instance inverters or PV simulators. However, in this study the complexities are put forth to have a HUT which is controlled from the virtual model by synchronized reference current signals based on power set-points and V_{pcc}. The idea behind is to analyze whether a single HUT (an amplifier) can behave dynamically as a source and sink, with controlled-current injections to feed-in and consume active/reactive power dynamically. Attempt is made through this study to operate the HUT in complete control as desired and what problems can occur to achieve this in a PHIL simulation. The thesis provides a base work to devise precise compensation algorithm for the CC amplifier as HUT based on the issues encountered.

1.1 Objectives

The primary objectives of this master thesis are three-folds:

- Firstly, the development of MONA LVDG in a complete phasor simulation environment. The phasor model should be compatible to be used for studying integration of distributed energy resources at low voltage distribution level.

    a. Inclusive in the above objective is the development of a simple hybrid load block that enables a bi-directional power flow. It should represent a realistic grid following inverter as a P-Q source behaving as a source and as a sink dynamically based on power setpoints. Additionally, a development of a smart inverter control block to model the state-of-the-art reactive power control strategies including volt-var behavior for the inverter.

- Secondly, the development of an effective hybrid simulation model completely in Simulink interface having part of the grid network modelled in discrete domain. It should depict proper representation of the phasor model via an equivalent circuit in discrete domain.

    a. This objective also extends to have an interface for generating reference voltage signals for the real-time simulator and for integrating feedback current of the HUT during real-time PHIL simulation.

- Lastly, the third and the final objective is to build a PHIL setup for a MONA low voltage distribution grid. Select an interface bus as a point of common coupling, the voltage at which is represented by a physical PI component i.e. the grid simulator (source) connected with the HUT (load).
    a. The above objective additionally involves the detailed characterization of the PI. The phase difference and errors between the reference real-time simulated voltage and the measured voltage.
    b. Develop a model to generate reference current signals for the HUT based on power set-points synchronized with the V_{pcc}. Evaluate the performance of the system with hardware as a current-controlled amplifier and as a constant resistive load bank.
    c. Develop compensation methods to improve the performance of CC amplifier as HUT. Highlight the complexities involved with the operation of CC amplifier as HUT. The limitations to operate it as an inverter with Q-management in a PHIL setup.

1.2 Thesis Outline

The structure of the thesis is further organized based on the following chapters:

Chapter 2; briefly discusses the theoretical aspects of hybrid simulation, why it is relevant for this thesis and other simulation techniques used to develop the grid model. Reactive power management from inverter-based generators is also discussed at length along with the detailed discussion on power hardware-in-the-loop approach, interface model and its applications.

Chapter 3; describes the development of the complete simulation model of the grid networks under study and the reactive power management functions for the modelled inverter block. Validation of the developed phasor model is performed. The scenarios implemented to test the grid model in complete phasor framework with Q-management functions and their results are also discussed in this chapter.

Chapter 4; In this chapter, the use of Simulink to develop a complete hybrid simulation model is proposed. The scenarios to be tested with the hybrid simulation model are also presented. To close up, the hybrid simulation results are presented to explain the functionality and relevance of hybrid simulation with respect to PHIL simulation.

Chapter 5: explains the development and approach related to the PHIL setup. The method to operate the setup is scripted in detail along with the scenarios to be implemented. The performance of the power interface and the hardware under test is illustrated with comprehensive results. The limitations and complexities towards testing the Q-management in a real-time PHIL setup is also discussed.

Chapter 6; Finally, concludes the thesis summarizing the main outcomes and optimization recommendations for future work.

2 Theory

2.1 Power System Simulation Approaches

In power system analysis, different approaches are adopted to study the stability of the system. The techniques implemented in this thesis are briefly introduced in this section.

2.1.1 Transient Stability Simulation

Due to the bidirectional power flow in modern distribution grids the stability and dynamics study is becoming increasingly important. Transient stability or phasor domain assessments plays an important role to perform grid integration analysis [10]. On the other hand, fully detailed electro-magnetic transient studies are very accurate but also poses computational processing limitations while examining large power systems. This is where time domain dynamic phasor models become attractive as they are less intensive computationally. It allows to implement large-scale power systems to study slow dynamics also referred as electro-mechanical oscillations pertaining to electrical machines i.e. generators and motors etc. But apart from studying the transient stability of electrical machines, it can also be implemented to observe the dynamic behavior involving amplitude and phase variations of voltages and currents.

The complex quantities in phasor simulation are subjected to slow variations that is why the time-steps used in the simulation are usually large compared to the EMT simulation, in the range of milli-seconds to seconds [11]. Therefore, the simulation is executed much faster representing the power system using a set of non-linear algebraic equations. Phasors of voltages and currents are being evaluated at each time step. The ability of the system to restore equilibrium by maintaining the voltage and frequency levels can be examined via this approach. This technique is suitable to study voltage fluctuations due to integration of distributed generators [12]. As the solution is computed at a single frequency, the variations in frequency are not much significant while simulating the power systems in phasor domain. However, work is being done to extend the dynamic phasor approach to model power systems with multiple and time-varying frequencies [11].

In phasor domain, the complex time-domain waveform x(τ) in the time interval τ ϵ (τ- T, t) is represented using a Fourier-series of the form as shown in **Equation(1)** [13]:

$$x(\tau) = \sum_{k=-\infty}^{\infty} X_k(t) * e^{jkw\tau} \qquad (1)$$

Where $w = \frac{2\pi}{T}$ and $X_k(t)$ is the k^{th} complex Fourier coefficient also referred as dynamic phasor. So, consequently in power system equations it would be voltage and current phasors. As already mentioned, this approach is suitable to conduct power flow analysis of large networks, therefore the impact of DER integration on the grid network is analyzed completely in phasor domain in this thesis. Multiple platforms are available for this purpose for instance ETAP, PSS/e, MATLAB-Simulink etc.

2.1.2 Electro-Magnetic Transient Simulation (EMT)

EMT simulation refers to the detailed modelling of the networks to analyze fast transients pertaining to power electronics in grids having inverter-based generation. The sample-time of EMT models are very low in the range of microseconds which means more accuracy, but the execution will be performed at a slower rate. In EMT simulation, the power system components are modelled using

continuous-time differential equations solved at each time-step [14]. It enables to obtain the fast-transient behavior but at the expense of high number of computations and time consumption.

The growing number of power electronics in the contemporary power networks increases the need for performing EMT simulation to capture fast transients. Therefore, this technique is suitable to study the effects of frequent switching of power electronic converters, Waveform distortions (harmonics, DC offset), switching frequencies, high frequency oscillations etc. Several tools are available to perform EMT simulation such as DIgSILENT PowerFactory, EMTP-RV, MATLAB-Simulink etc. However, only the portion of the power system which is of interest is simulated in EMT domain due to low execution speed [15].The same approach is adopted in this thesis by modelling only part of the system in EMT domain, the details are presented in **section 4.1**. The following **Figure 2.1** shows the timeline for time-steps usually considered while performing simulation studies to represent sufficient dynamics of a power system.

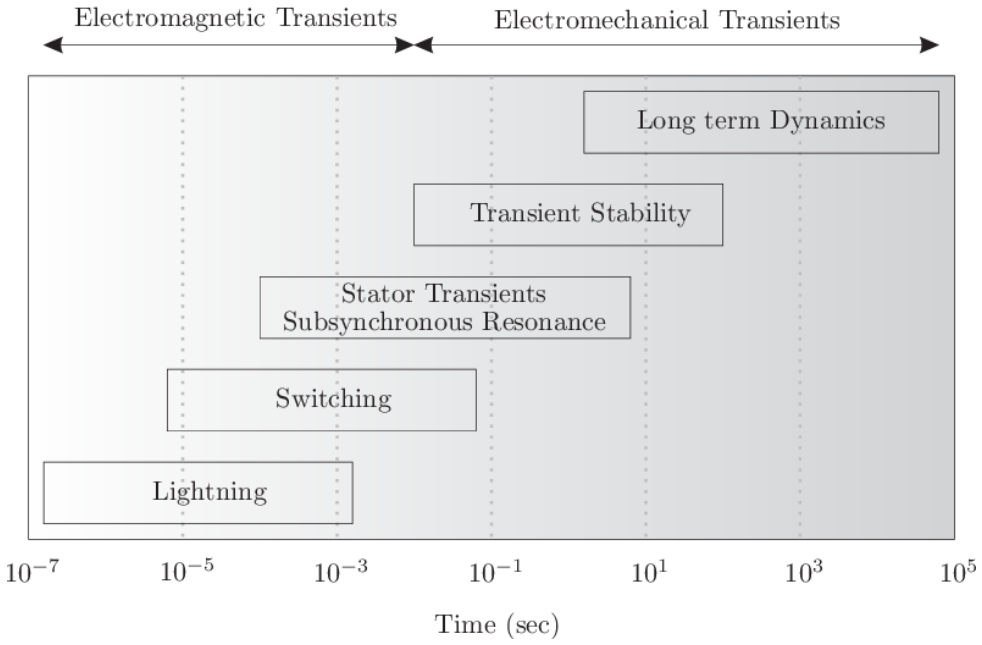


Figure 2.1. Time frame for power system transients [16].

As shown in the **Figure 2.1** above, for events involving fast transients switching, lightning etc. the timesteps are very low. Voltage stability and power flow analysis fall more towards the right side of the time frame under transient stability and long-term dynamics having higher time steps.

2.1.3 Hybrid Simulation

As phasor simulation technique has limitations in portraying detailed transients of the systems and EMT simulation for large networks is not viable, an approach is desired which has both low computational demands and high accuracy. Hybrid simulation phenomena serves this purpose. A lot of research has been carried out on studying EMT-TS hybrid simulation approaches to define interfacing practices [17] and equivalent sub-system circuit models representation on both sides [18] [19].

Hybrid simulation as its name implicates allows to model a large section of the network in phasor domain with power flow equations solved at fundamental frequency while a part of the network with a detailed model is simulated in EMT domain. It is solved using differential equations [15]. Also, the

simulation in both the domains can be carried out at different sample-times. So, two sub-systems are simulated, one at a large time-step (Phasor) and other at a very low time-step (EMT or discrete).

For communication between the two sub-systems the boundary conditions and network variables must be transformed from one simulation platform to another. The following **Figure** 2.2 illustrates the basic structure for two sub-systems interfaced to each other when simulated in different domains.

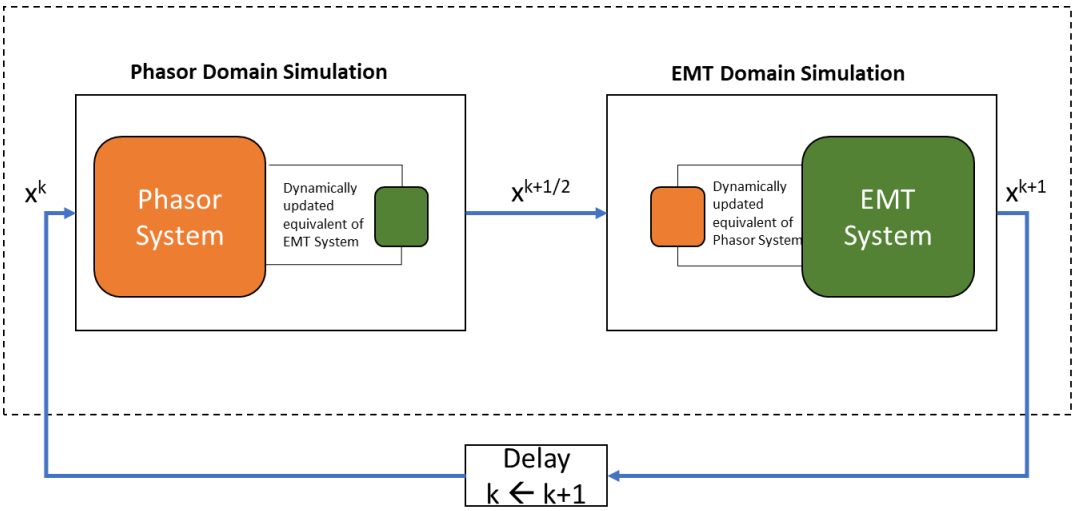


Figure 2.2. Model of one system dealing with the other during hybrid simulation. Modified from [9].

One of the equivalent sub-system circuit approach found in literature [18][19][10][9] and also adopted for this thesis is illustrated below in **Figure 2.3** . More details regarding the development of the hybrid model and sub-system equivalents are provided in **section 4.**

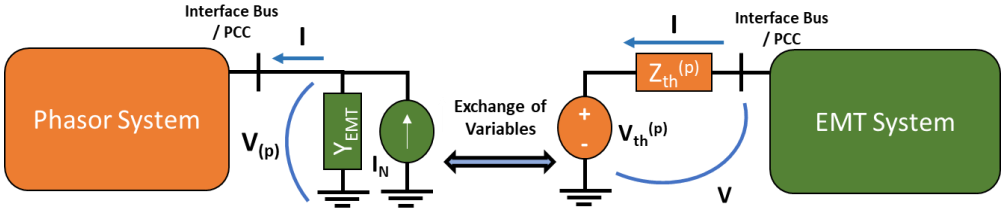


Figure 2.3. Equivalent sub-system models.

As shown, Thevenin and Norton equivalent models are used in each of the sub-systems. In phasor domain, time-varying Norton equivalent circuit is used to represent the EMT system at the interface bus. In EMT domain, time varying Thevenin equivalent circuit is used to represent the phasor system at the interface bus. The choice of equivalent circuits are interchangeable [18]. To improve the accuracy of the simulation it is important to have precise updated variables for the equivalent circuits in both the sub-systems. For this the data at the PCC is extracted dynamically during the simulation.

2.1.3.1 Data Extraction and Interaction

As both the sub-systems are coupled, the output from one of the sub-systems is transmitted as an input for the other. Desired equivalent circuit values including impedance, voltage amplitude, voltage phase angle and frequency are required to be extracted dynamically at each time-step. Firstly, in EMT domain the values from the phasor domain at the fundamental frequency is transformed into a waveform. Secondly, the phasors (magnitude and angle) are extracted from waveforms in EMT domain

using Fast Fourier Transform at the fundamental frequency before feeding the values back to the phasor domain sub-system [10]. Data must be transformed into appropriate forms before exchanging between the two sub-systems as shown in the **Figure 2.4** below:

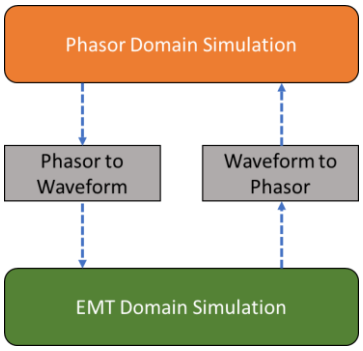


Figure 2.4 Data exchange between the two simulation domains.

Similarly, the Thevenin equivalent impedance for phasor sub-system representation in EMT domain needs to be calculated at the interface bus in phasor domain in order to update the Thevenin voltage source [9]. Mathematically , it can be represented as the following **Equations(2)** and **(3)** modified from source [10] using subscripts as shown in **Figure 2.3**.

$$Z_{th(p)} = R_{th(p)} + j * w_s * L_{th(p)} \tag{2}$$

$$V_{th(p)} = V - I * Z_{th(p)} = V_{th(p)} * e^{j\theta} \tag{3}$$

Where $Z_{th(p)}$ is the equivalent Thevenin impedance representing the phasor domain sub-system , $V_{th(p)}$ is the Thevenin voltage source value in EMT domain, V and I are the voltage and current values at the interface bus. Likewise, for the respective Norton equivalent circuit in phasor domain the current injection can be mathematically defined as shown in **Equation(4)** modified from source [10] using subscripts as shown in **Figure 2.3**.

$$I_{N(EMT)} = V_{(p)} * Y_{(EMT)} + I \tag{4}$$

Where $I_{N(EMT)}$, is the current injection value for the Norton current source in phasor domain, $V_{(p)}$ and I are the voltages and currents at the interface bus [10]. The impedances would remain the same until and unless there is a change in the network in the phasor domain sub-system for instance faults, short-circuit or in the EMT domain sub-system for instance switching [20].

For interaction between the two sub-systems there is a need for an interaction protocol. The protocol ensures smooth operation between the two models simulated at different timesteps. The two renown interaction protocols found in literature are the serial and parallel protocols. In order for the hybrid simulation to run in real-time, both the models must be involved simultaneously and that is achieved in parallel protocol [21]. The following **Figure 2.5** shows the hierarchy followed during the parallel interaction protocol.

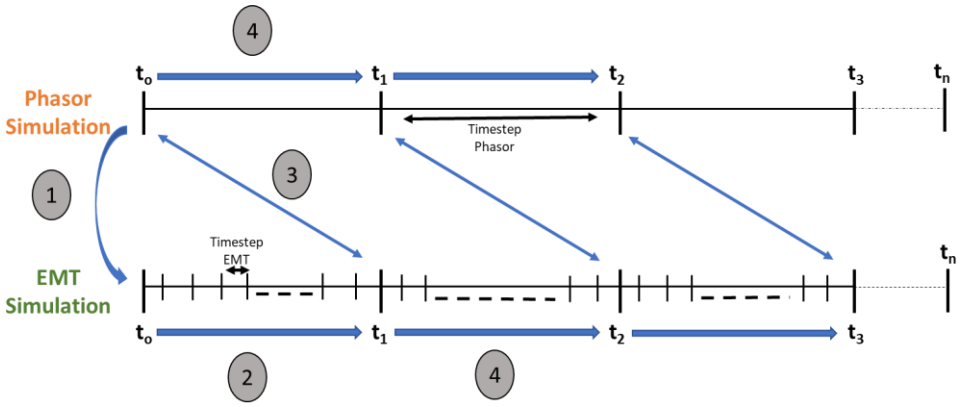


Figure 2.5 Parallel interaction protocol. Redrawn from [17].

The iterative procedure is explained briefly below:

- Each sub-system simulation starts at the same time. From phasor model, the values of Thevenin equivalent voltage sources are transferred to the EMT model at time t_o.
- EMT model is simulated until the next time-step t_1 based on the equivalents obtained from the phasor model.
- In EMT domain, phasor values are obtained at the interface bus for Norton equivalent current sources. The values are transferred at t_1 back to the phasor model.
- The updated equivalents from EMT model are received with a delay by the phasor model at t_o. Both the models then advance to the next time-step. Phasor model to t_1 and EMT model to t_2.
- The steps 3 and 4 are repeated until the simulation is executed for the total time.

Thus, both the sub-systems are simulated continually and does not remain idle while following the parallel interaction protocol.

2.1.3.2 Relevance of Hybrid Simulation for PHIL in this Thesis

The real-time simulator utilized in this thesis requires a waveform of the electrical signals (voltages / currents) discretized at a high sample rate which is then converted to analog signals for power amplifiers. Therefore, the hybrid simulation approach deems accurate as part of the grid model simulated in EMT domain can provide the desired discrete waveforms. The phasor domain only provides the phasors (magnitude and angles) which needs to be transformed to discretized waveforms to be processed by the real-time target machine. That is why a small part of the distribution grid is modelled in discrete domain which provides the waveform at the interface bus. These signals can be fed into the real-time simulator. Similarly, the feedback currents can also be treated in the discrete domain and integrated into the grid model. However, a detailed EMT model of a PV system is not utilized in this thesis as the scope of the thesis is not to analyze power quality of the grid. The main purpose behind implementing hybrid simulation is to acquire precisely synchronized transformed waveforms from phasor domain and integrate current feedback signals to the close the PHIL simulation loop.

MATLAB-Simulink is used to implement the hybrid simulation, as the whole framework can be implemented on a single platform rather than using individual TS and EMT tools. Also, the interfacing and the exchange of data between the two models becomes less complex. The powergui (power graphical user interface) block in Simulink enables to simulate one sub-system in phasor domain while

the other in discrete domain with much lower sample-time. The method is scripted in detail in **section 4.**

2.2 Reactive Power Management

In compliance with Germany's Erneuerbare Energien Gesetz §8 EEG 2017 [3], the distribution system operators are bound to integrate renewable energy based generators in the grids. Similarly, in compliance with §12 EEG 2017 [3], if the distributed generation capacity cannot be added to the grid due to technical constraints, the grid operators are obliged to execute necessary grid reinforcements. With these regulations intact, the operators have to linger over possible technical frameworks to interconnect increasing roof-top PV systems while maintaining the quality of electrical supply.

Distributed generation integrated into the power grids also have to participate in maintaining resilience of the network by providing controls as defined in German LV guidelines for interconnection of DG [4]. Reactive power provision through grid interfaced inverters is one of the measures for voltage regulation. It can support the local grid voltage by consuming or injecting reactive power. This phenomenon is also very common in conventional grids. By controlling the reactive power, the voltage profiles of the grid network can be maintained within permissible limits [22]. With increasing commercial / residential PV deployment, the inverters interfacing grids are now being utilized to provide reactive power control under defined regulatory frameworks.

2.2.1 German Low Voltage (LV) Grid Reactive Power Provision Regulations

As a low voltage network is studied in this thesis, only guidelines pertaining to LVDG are discussed. In Germany, the technical guidelines for LV network [4] states that all PV systems must be capable of providing reactive power and has set certain requirements. The following **Table 1** summarizes these requirements for PV systems of different sizes in Germany at LV grid level:

Table 1. Power factor settings according to the technical guidelines for distributed generators connected to LVDG [23].

Voltage Level	PV System size	Minimum Power Factor	Power Feed-In
Low Voltage	S < 3.68 kVA	No requirements	-
	3.68 kVA ≤ S ≤ 13.8 kVA	0.95 leading / lagging	P(t) ≥ 20 % of S
	S > 13.8 kVA	0.90 leading / lagging	P(t) ≥ 20 % of S

Thus, it can be extracted that the provision of reactive power should be made possible for systems having an apparent power greater than 3.68 kVA.

2.2.2 Reactive Power Influence in Power Grids

Grid connected inverters are the core elements of DER. At present, a lot of work is being carried out in terms of providing voltage support by active and reactive power control of grid connected inverters. Voltage support by DG (for instance: PV inverter) can be understood by the following equivalent circuit of a distribution grid with PV inverter as shown in **Figure 2.6** and the following voltage change equations explained in study report [5].

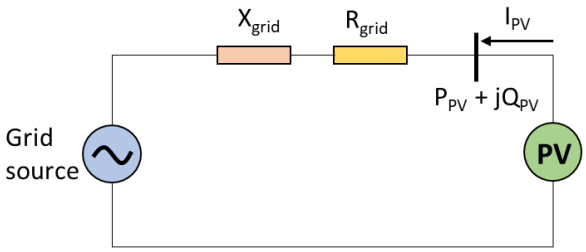


Figure 2.6 Schematic of PV connected to the grid.

Change in voltage at PV connection point is given by **Equation(5)**. Rearranging, **Equation(5)** by taking the active power part (R*P) and (U_{grid}^2) common produces **Equation(6):**

$$dU \approx \frac{(R * P) + (\mp Q * X)}{(U_{Grid})^2} \tag{5}$$

$$dU \approx \frac{R * P}{(U_{Grid})^2} * [1 + tan\emptyset * \frac{1}{\frac{R}{X}}] \tag{6}$$

Where R, P, Q, X and φ represents resistance, active power, reactive power, reactance, and power factor, respectively. From **Equation(5)** it can be seen that the voltage at the PCC will rise when the active power feed-in increases. On the other hand, reactive power (lagging or leading) can be used to control the voltage deviation. From **Equation(6)**, it can be observed that reactive power depends highly on the (R/X) ratio of the distribution network. The larger the ratio, the more reactive power would be required to compensate the increase in voltage.

All distributed generators connected to the distribution grid are supposed to provide reactive power through power inverters as defined in guidelines shown in **Table 1.** In this study, a maximum reactive power limit for a power factor of 0.9 is selected in order to represent the reactive power provision capacity of inverters deployed at low voltage level. **Equations(8)** and **(9)** are used to evaluate the maximum power in-feed and reactive power at a certain power factor. Whereas, the limitation of general reactive power supply by an inverter is governed by the **Equation(10)** [24].

$$S = P + jQ \tag{7}$$

$$P = S * \cos\emptyset \tag{8}$$

$$Q = S * \sin\emptyset = \frac{P}{\cos\emptyset} * \sin\emptyset = P * \tan\emptyset \tag{9}$$

$$|Q| \leq \sqrt{S^2 - P^2} \cong Q^{max} \tag{10}$$

Where S is inverters rated apparent power, P is inverters generated power, Q dictates the reactive power limit of the inverter while supplying a certain amount active power and cosφ is the power factor. The following **Figure 2.7** illustrates the max reactive power limit range as implemented in this thesis for the rated apparent power (S) and maximum power feed-in(P).

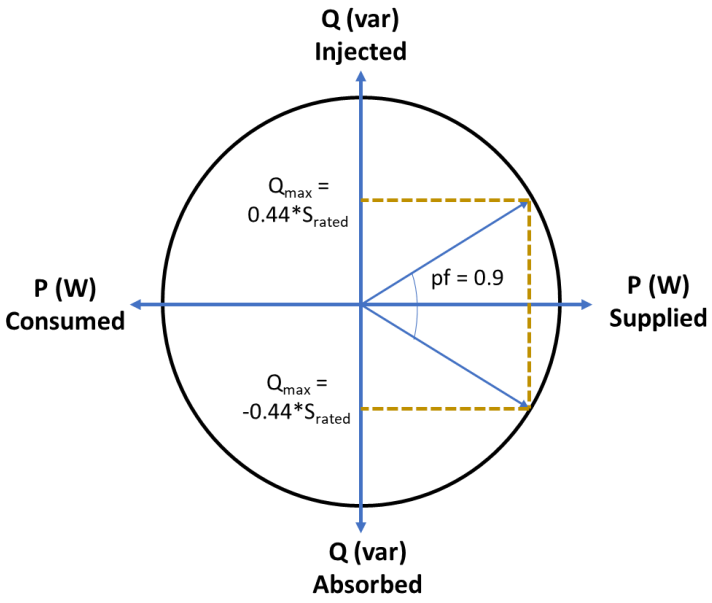


Figure 2.7 Reactive power limits for modelled inverters.

Different Q-control approaches are being proposed in literature as discussed in the following **section 2.2.3**. For low voltage distribution grid networks, the applications of central reactive power control approach would require establishing highly reliable communication channels and intensive computational power to be done in real operational time. Whereas, local approach applied to each inverters should be fine-tuned to achieve desired voltage support [25]. Therefore, the approach applied by DSO can vary even if they are operating in the same country [5]. State-of-the art Q-control strategies implemented in this thesis are discussed in the following section.

2.2.3 Reactive Power Control Strategies

The reactive power provision control method could be static or dynamic. Static approach is used to maintain the voltage levels during normal grid operations (reactive power changes in time period of seconds to minutes) while dynamic approach is desired to handle sudden voltage drops (reactive power output changes within milliseconds). This technique is mostly utilized at high or medium voltage levels when the utility scale PV systems contribute towards fault ride-through i.e. collapse of grid voltage [26].

Currently most of the PV inverters have the capability of providing static reactive power however its practical utilization is up to the local DSO who makes the decision based on the dynamics of the grid operation. It is difficult to state categorically that a uniform method for reactive power provision exists among DSOs. Nevertheless, the common reactive power control methods being implemented are[5]:

- Constant power factor; supply of reactive power to the grid with a constant ratio of active and apparent power.
- Regulating reactive power as a fixed characteristic curve as function of voltage Q(U); commonly known as volt-var control. Characteristic curve can be adjusted by grid operators.
- Regulating power factor as a function of active power cosφ(P); known as watt-power factor function.

Thus, above defined reactive power control strategies are the same being tested in this thesis. The following **Figure 2.8** illustrates the example of cosφ(P) and Q(U) characteristic curves:

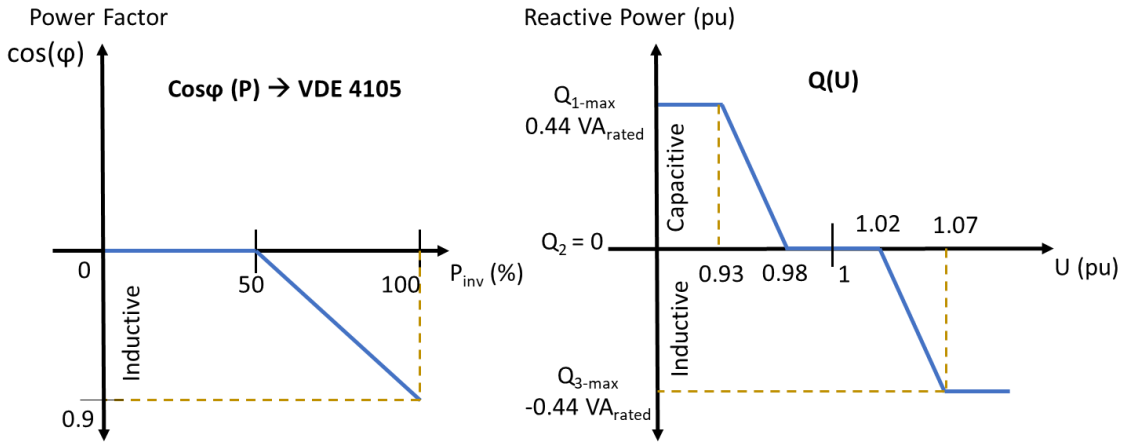


Figure 2.8 Cosφ (P) characteristic curve (left) and Q(U) characteristic curve (right) implemented for this study.

For Q(U) graph shown in **Figure 2.8**, it can be observed that when the per unit voltage at the PCC is less than or equal to 0.93 pu, the inverter would inject the maximum reactive power(Q_1) to raise the voltage. While between 0.93 pu and 0.98 pu, the amount of reactive power injected by the inverter will be controlled by the equation stated below based on the V_{pcc} at that time instant. In between 0.98 and 1.02 pu is the dead-band which means no reactive power would be injected or absorbed in this voltage range. Similarly, when V_{pcc} is between 1.02 pu and 1.07 pu the reactive power will be absorbed to limit the voltage rise. Finally, when V_{pcc} reaches at 1.07 pu or beyond maximum reactive power(Q_4) will be absorbed. The corresponding slope equations shown in **Figure 2.9** are used to define the reactive power value at different voltage set-points.

$$Q(U) = \begin{cases} Q_1 & U \le 0.93 \\ \frac{Q_2-Q_1}{0.05} * (U) + Q_2 - (0.98) * \frac{Q_2-Q_1}{0.05} & 0.93 < U \le 0.98 \\ Q_2 & 0.98 < U < 1.02 \\ \frac{Q_3-Q_2}{0.05} * (U) + Q_2 - (1.07) * \frac{Q_3-Q_2}{0.05} & 1.02 \le U < 1.07 \\ Q_3 & 1.07 \le U \end{cases}$$

Figure 2.9 Equations governing volt-var function [27].

Based on the operating scenarios of the network, different control strategies are opted by local DSO. The sole objective is to provide voltage control and increase the hosting capacity of distributed generation. Another challenge that lies within the volt-var approach is defining the characteristic curve. An assessment of 17 real LV grids in PhD dissertation [28] already depicts that the choice of set-points for reactive power have significant influence on the performance and hosting capacity of LV grids. However, optimal characterization of volt-var curve Is not in the scope of this thesis.

2.3 Real-Time Simulation

The decentralization of power grids with customer-side contribution to the power flow would require automation, control, monitoring and demand-response abilities to continue reliable power supply to the grid. To test the response of power systems in accordance with mentioned objectives, the real-

time simulation provides a suitable platform. It allows validating novel DER integration approaches so that technical issues can be solved conveniently to achieve modernization of the power grids.

2.3.1 Power Hardware-in-the-Loop

Power Hardware-in-the-loop (PHIL) and Hardware-in-the-loop (HIL) concepts incorporates real-time conditions, as actual signals are transmitted through a power interface, respectively. The PHIL simulations are widely used for analyzing and validating power system components specially pertaining to smart grid concepts. A general PHIL system architecture is depicted in **Figure 2.10** below.

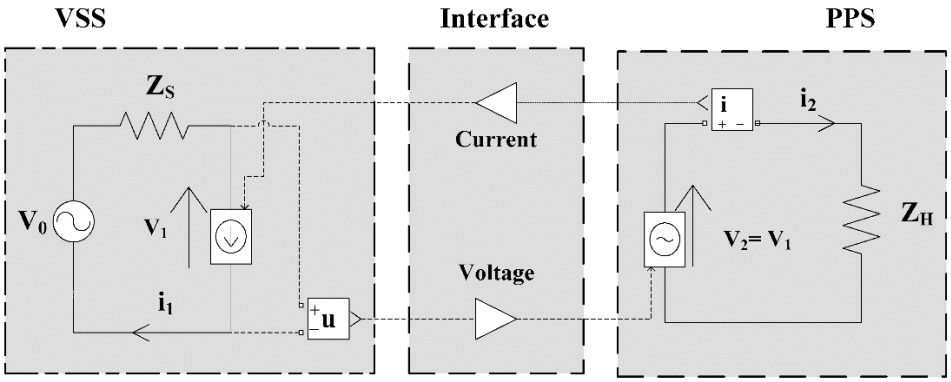


Figure 2.10 General power hardware-in-the-Loop (PHIL) system architecture [29].

The VSS represents virtual simulated system indicated by a voltage source (V_o) and internal impedance (Z_s). The measured voltage V_1 obtained in the VSS is transmitted through the interface to physical power system (PPS). The PPS is represented by a controlled voltage source and the hardware impedance (Z_H). The voltage signals are amplified by means of a power amplifier [29]. Parameters of interest (i.e. measured current i_2) of the hardware is sent back to the simulation environment (VSS) through a current-controlled source.

A PHIL setup requires a power interface to transmit signals (voltage / current) from the simulated environment to the real hardware and vice versa. Stable operation of PHIL setup is ensured by means of an interface to minimize the influence of measurement probes and power amplifiers on system dynamics [29]. In referenced studies [29][30], the common interface algorithms for PHIL setups are discussed in detail. However, in this thesis the basic structure with an Ideal Transformer Model - voltage type interface as shown in **Figure 2.11** below is adopted. The modelled grid is represented by an equivalent voltage source and impedance, the grid node voltages are sent to the power interface connected to the HUT. As a feedback, the current drawn by the hardware is measured and sent back to the grid model simulated in real-time though a controlled-current source.

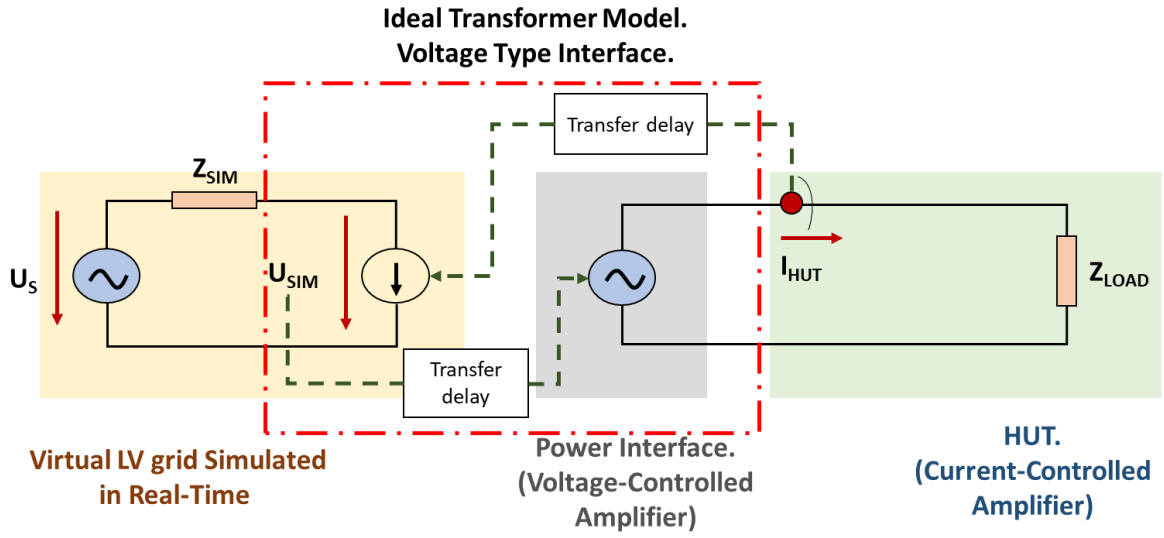


Figure 2.11 Ideal transformer model -ITM (voltage type) PHIL interface. Modified from [31].

2.3.1.1 PHIL Characterization and Stability

Some of the characteristics important to be considered while opting for suitable amplifier for PHIL applications are defined below [32]:

- Power ratings of the hardware under test (HUT).
- Input and output (Voltage / Current) range of the power amplifier.
- Response times of the power amplifier.
- Amplifier protection (short circuit events, overload, overvoltage).

Time delays in PHIL operation is also a major issue that can lead to instability and inaccuracy of the complete setup. It can comprise of the following [32]:

- Time delay in sending the simulated V_{pcc} to the power interface by the real-time simulator, depicted by U_{SIM} in **Figure 2.11.**
- Time required by the amplifier to produce the amplified output voltages at its terminals.
- Time required by the feedback signals to be sent back to modelled virtual grid via real-time simulator, depicted by I_{HUT} in **Figure 2.11.**

Due to the time delays, the measured output values of the amplifier at the same time instant would be different than the reference values sent to the amplifiers. The total loop delay from the sent-out voltages to the obtained feedback current is shown by the following **Equation(11).**

$$\tau = \tau_{AMP} + \tau_{RTS} \tag{11}$$

Where, τ_{AMP} is the time elapsed between, when the values are transmitted to the amplifier and when it returns the corresponding (voltage / current) measurements. τ_{RTS} Is related to the computation and communication intervals within a given sample-time of the real-time simulator [32]. Details about RT system, Power amplifier, and HUT used in this study are provided in the following section.

2.3.1.2 PHIL System Components Description and Functionality

The PHIL system comprises of three main parts [33].

- **Hardware under Test (HUT):** It is the equipment in the setup, the operation of which is to be examined. For this thesis, the main HUT is a switched mode 30 kVA AC source operating in current-controlled mode from Regatron AG® of type TopCon TC.ACS. This series from Regatron AG supports the operation of current controlled amplifiers in both 'Feeding Mode' for positive power and 'Regenerative Mode' for negative power [34]. This characteristic is quite helpful while performing PHIL studies for DER integration. As the HUT can serve as a hybrid load, operating as a load and also as a feed-in source dynamically based on the power set-points. For one scenario, a constant resistive load bank is also used as a HUT.

- **Power Interface (PI):** This element in the setup enables to get the operating points of a real electrical power system from the simulated environment and makes it available in the real world (for instance: voltage at the PCC). The power interface in this study is a switched-mode voltage source, a 50 kVA 4-Quadrant grid simulator from Regatron AG also of type TopCon TC.ACS operating in voltage-controlled mode [34]. It behaves as a grid simulator representing the voltage at the PCC. Technical datasheets of both the power amplifiers used in this study are provided in **Appendix B**.

The TC.ACS amplifiers have built-in protection features programmed to prompt circuit breakers in case of phase overcurrent, over voltage etc. leading to electrical isolation of the device. The basic circuit for both current-controlled and voltage-controlled amplifiers is illustrated in **Figure 2.12** below.

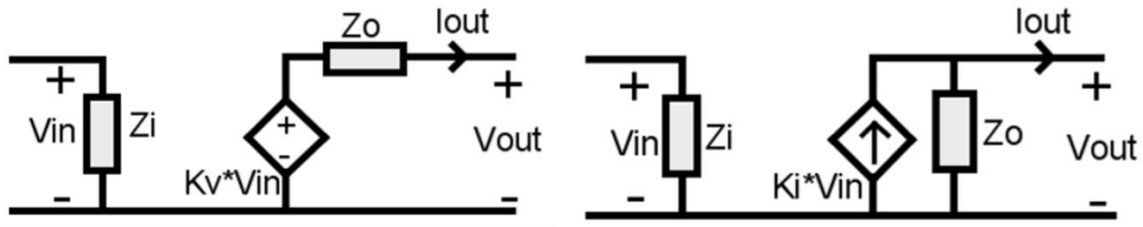


Figure 2.12 Voltage-Controlled amplifier (left) and Current-Controlled amplifier (right) [32].

The voltage-controlled amplifier on the left is represented by a voltage source with an output impedance in series, V_{out} is the voltage available across the output terminals of the amplifier. The current-controlled amplifier on the right is represented by a current source with an output impedance in parallel, I_{out} is the current being injected into the circuit by the amplifier.

- **Real-Time Simulator (RTS):** The real-time simulator simulates the grid model in real-time and performs digital-to-analog conversion of electrical signals and vice versa. It transmits the scaled down analog values (i.e. V_{pcc}) from the simulation environment to the power interface and from the HUT (e.g. current) back to the simulation environment. In this thesis, Speedgoat real-time target machine® is used as a RT simulator with the mathematical grid model developed in Simulink built on its multi-core processors.

In general, concerning the RT digital simulators various emulator options are currently being utilized. Some of the most popular RT simulators with their applications and software interfaces are defined in the **Table 2** below.

Table 2. Real-time simulators. Modified from [35].

Simulator	Software Interface	Applications
Opal-RT	MATLAB, Simulink, Labview	Power electronics, control systems, HIL, power systems, smart grids
RTDS	MATLAB and Simulink	
Speedgoat RT Target Machine	Simulink, MATLAB	
NI Hardware	Labview	
Typhoon	MATLAB	Power electronics, control systems, HIL

In the context of smart grid controls, not much literature is found in which Speedgoat RT target is being used as a RT simulator. The use of Regatron devices as grid simulators / power interface is quite common though. The application of Regatron device as a PI is discussed in [33] to test smart-grid controls. The software tool DIgSILENT PowerFactory has been used as a virtual environment passing V_{pcc} to the Regatron's voltage source interfaced to the HUT (i.e. a commercial inverter). In another study [36], Regatron's PV simulator is used, integrated with a battery emulator to test energy storage applications. The control system has been implemented in Simulink environment. Similarly, in [31] a PHIL setup is implemented to validate the developed battery-model in real-time using Regatron's amplifier as a power interface.

2.4 Summary

From the discussion in this chapter it is evident that the autonomous reactive power provision practice is mandatory at LV level and inverters are contributing towards voltage regulation in power grids. For a complex system, real-time testing of power components in a controlled environment is a key element. With the rise of DER and digitalization process, the need is to develop a method for PHIL testing and communication of inverters with defined benchmark systems. It will prove to be an efficient mechanism to observe and validate smart inverter management strategies. This will also help the DSO to observe the viability of Q-management in low voltage distribution grid in real-time.

3 Development of Simulation Testbed (Grid Models)

The complete phasor model of the grid networks, its validation and simulation results are presented in this chapter.

3.1 MONA - Low Voltage Distribution Grid Networks

The two radial low voltage distribution grid networks being considered in this thesis are MONA – 8002 and MONA – 8008 from the MONA Project 2030 [37]. Single-line diagram of both the networks are shown in the **Figure 3.1** below.

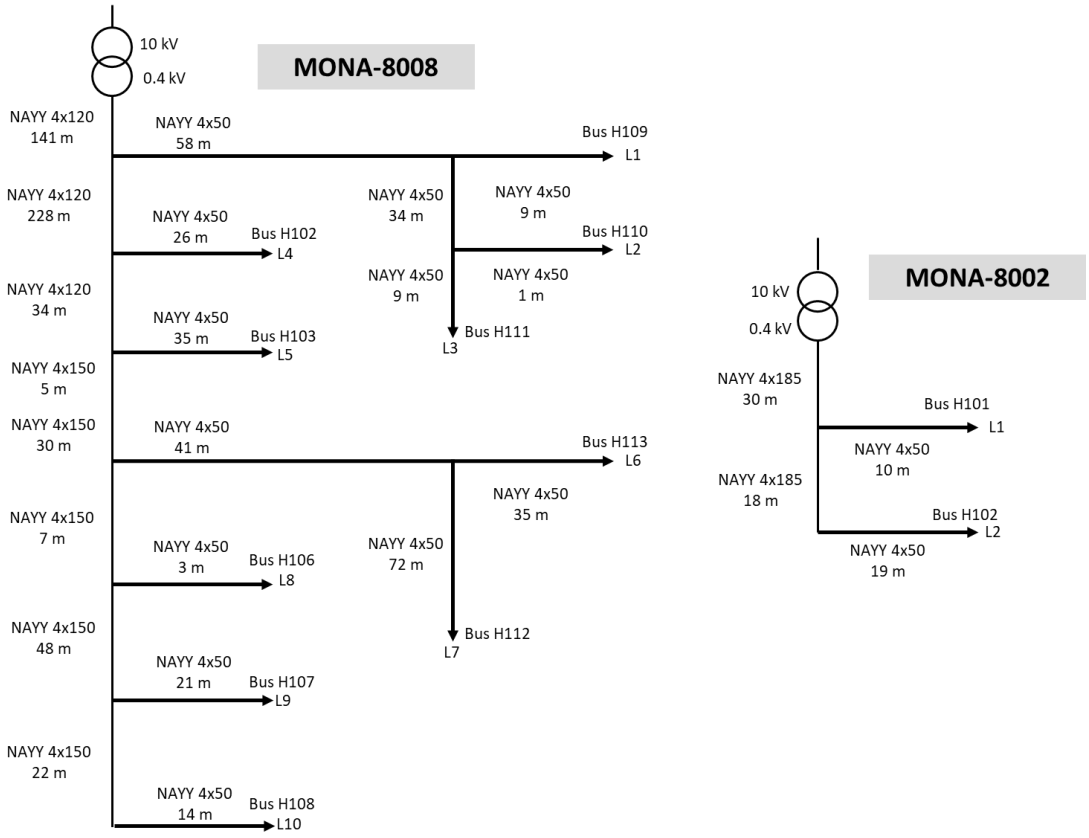


Figure 3.1 LVDG networks [37].

NAYY represents the line codes in OpenDSS™ [38] (an opensource power distribution system simulator) format with a number representing the cross section of the cables. L represents the loads connected to respective buses. Details about distribution line parameters (length, resistance, reactance) and step-down transformer is provided in the **Appendix A** and also can be accessed at the project source[37]. The structure of MONA-8002 grid is quite simple with a single step-down LV transformer and two load nodes, while MONA-8008 is a bit complex compared to MONA-8002 and has 10 load nodes. The MONA-8002 network is mostly used for validation and in real-time PHIL test in this study, while impact of feed-in and Q-control strategies is analyzed in detail for MONA-8008 network. The base voltage levels of the networks are 10 kV and 0.4 kV.

3.1.1 Load and PV Profiles

The load profiles being utilized in this thesis are taken from the publication database of HTW-Berlin [7] having 74 different load profiles and PV profile is also from the HTW-Berlin database source [8].

The SP load profiles (active and reactive power) are provided with a temporal resolution of ~1s and ~1min. In simulation studies of MONA-8002 LV grid, for each of the loads a different SP load profile is implemented to depict real consumption of a LV grid. For simplicity, in cases where a TP load is modelled the active and reactive powers for each of the phases (A, B, C) are added and then utilized as a TP load profile.

In simulation studies of MONA-8008 LV grid, to have a balanced system and for the convenience of per phase analysis the same SP daily load profile with a temporal resolution of 1 min is integrated for all the phases of a certain bus. Thus, the network analyzed is a TP balanced LV network. For the PV profiles, the same SP profile is implemented for each of the feed-in units modelled. However, to add a dynamic element in the feed-in behavior the profile is first normalized and then multiplied by a feed-in factor generated randomly between the range of 1-10 kW for each of the buses. The reason for choosing this range is the fact that majority of the PV systems at low-voltage grid level in Germany have an installed capacity in between 1-10 kW and around 90% of PV systems have an installed capacity of under 30 kW [1]. Therefore, the highest SP peak feed-in power for the PV unit modelled is equal to or below 10 kW which would render to a maximum total TP capacity of 30 kW at one bus. As MONA-8008 network has 10 nodes, 10 feed-in factors are randomly generated to be multiplied with the normalized PV-profile. The factors are tabulated below for each of the buses. Bus tags are taken as indicated in the MONA grid database and also shown in **Figure 3.1**. Also, the load profiles integrated in MONA-8008 simulation studies are indicated with a load profile number corresponding to each bus as taken from HTW-Berlin database.

Table 3. Feed-in factors for normalized PV profiles and load profiles integrated at each bus.

Bus No	Feed-in Factor (kW_p/phase)	Load Profile No
H102	6.8	1
H103	8.2	2
H106	5.1	3
H107	4.9	4
H108	8.4	5
H109	1.8	6
H110	2.2	7
H111	2.6	8
H112	4.5	9
H113	8.5	10

The node farthest from the sub-station step-down transformer is Bus H108 in MONA-8008 refer **Figure 3.1.** The reactive power management strategies are tested on this node. It also has a high feed-in with 8.4 kW_p/phase refer **Table 3** above. As the PV profile used is for a SP, the same is integrated at all the three phases to have a balanced TP PV integration. The **Figure 3.2** below shows the SP power profiles of load and PV at Bus H108.

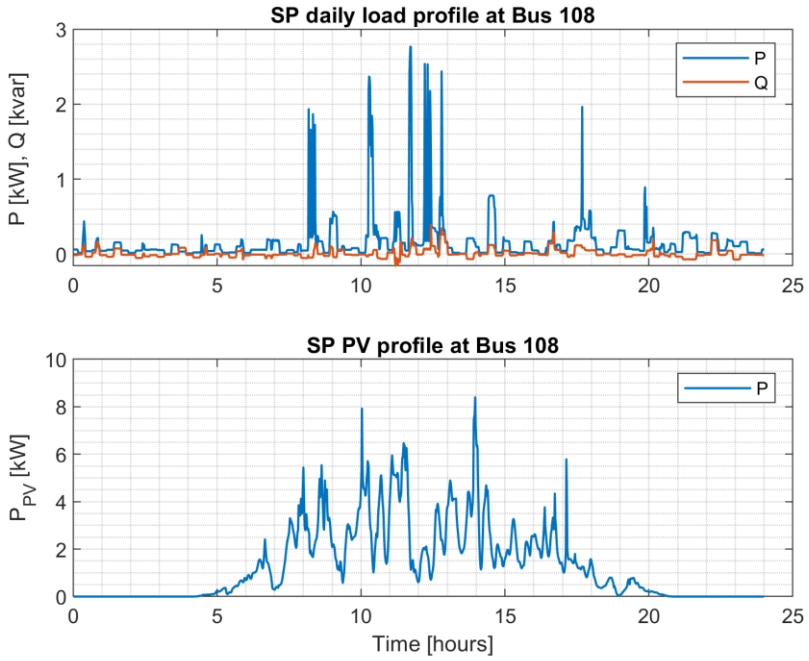


Figure 3.2 Load and PV profile integrated at Bus H108.

3.2 Modelling of the MONA Grid Network

The Simscape-Electrical, Specialized Power Systems (SPS) toolbox is used to model the grid networks in Simulink platform. The power source and the S/D transformer are accumulated into a sub-system representing the utility. Three-Phase Source block in swing mode at base voltage (10 kV) is used as the main power source. Similarly, the Three-Phase Transformer (Two-windings) block is used to model the S/D distribution transformer. The lines are modelled using the Distributed Parameters Line block connected to the Load Flow Bus (LFB) blocks. The LFB blocks indicates all the buses in the LV network, additionally each of the loads are connected to these buses with a unique bus identity. Three-Phase VI measurement block is used to measure the voltages / currents at each of the load buses. The **Figure 3.3** below illustrates the grid model of MONA-8002 developed in Simulink using blocks from SPS toolbox.

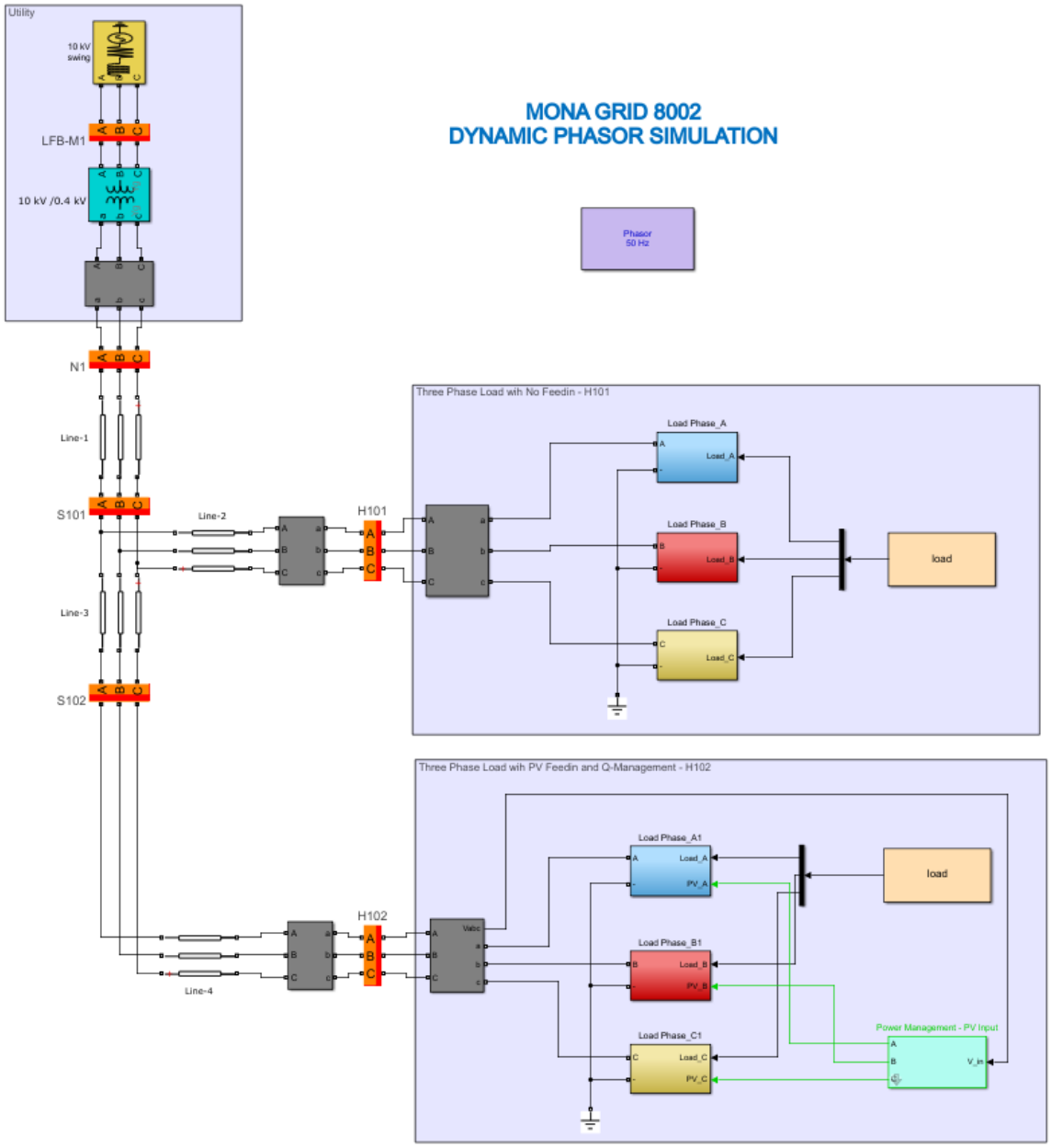


Figure 3.3 MONA-8002 LV grid model in Simulink-MATLAB phasor domain.

At Bus H101, a load is connected having three SP dynamic load blocks whereas at Bus H102 in addition to the load blocks a power management block is connected. This block represents PV feed-in and is also incorporated with Q-control strategies. Details of the respective model blocks is provided in the following section.

3.2.1 Load and PV Model

The model blocks used to represent the load and feed-in unit are explained in this section.

3.2.1.1 Load Model

For modelling of the loads three approaches are being used based on the application as described below:

- **Three-Phase Constant Load:**
  To model a constant load consumption, TP RLC load blocks are used which enables to specify combined or separate per phase active and reactive (inductive / capacitive) power demands.

- **Three-Phase Dynamic Load:**
  To implement a dynamic load the Three-Phase Dynamic Load block is implemented. By default, the powers absorbed by the load vary as a function of positive-sequence voltage, but the powers can also be provided via an external control. The load power profile time series is provided as an array of *[Time, P, Q]* via the From Workspace block.

- **Single-Phase Dynamic Load:**
  For implementing a simple single-phase dynamic load current-controlled sources are used for each phase. The current signals for which are calculated based on the phase voltage and the defined active and reactive power from the load profiles. The following circuit in **Figure 3.4** illustrates a simple SP dynamic load modelled using a controlled-current source and a high impedance in parallel interfaced with the grid.

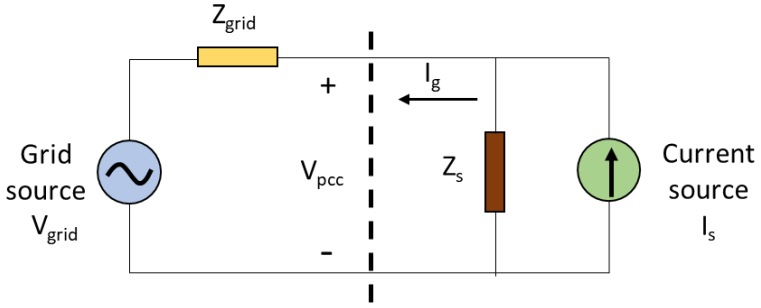


Figure 3.4 Equivalent circuit for SP load - grid / inverter-grid connection.

3.2.1.2 PV Model

The level of detail for PV model is also very important when performing power flow studies. For this study, the goal is to develop a simple model of PV inverter for low-voltage grid suitable for studying the power injections by the inverter at the PCC. Therefore, the PV inverter is modelled simply as a P-Q source as the main interest is not towards studying the transients or dynamics related to power electronics but rather towards implementation of Q-management of an inverter in real-time. It is basically the same as SP dynamic load block referred as an impedance model (a current source with a parallel impedance) as shown in **Figure 3.4,** to represent a grid-connected inverter. The sign of the active power set-points will define the functionality of this block as an inverter or load. The idea behind is to model a grid following inverter with grid support function (for instance voltage regulation) which injects synchronized current at the grid connection bus based on the power setpoints. The following **Figure 3.5** illustrates the complete control flow for grid following inverters.

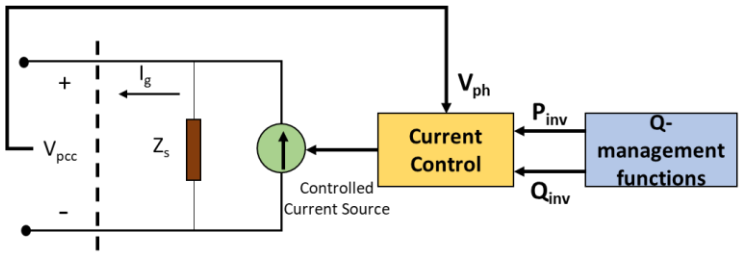


Figure 3.5 Grid-following inverter with Q-management support functions. Modified from [39].

As stated, it is the same as the SP dynamic block represented by a current-source and an impedance as shown in **Figure 3.4**. The above model is used for a single-phase PV unit but for implementing the TP PV unit as a simple inverter the Three-Phase Dynamic Load block from Simulink can be used. The only difference is the sign of external power signal provided to the block. Averting the values from positive to negative of active power time series input will make the block operate as a feed-in source rather than a load. The following **Figure 3.6** illustrates the idea.

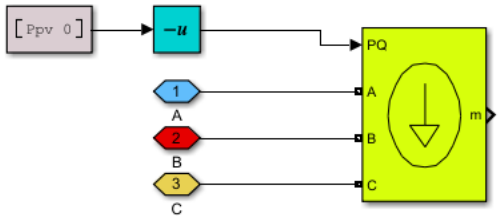


Figure 3.6 TP inverter using Simulink dynamic load block.

3.2.2 Hybrid Load Model

As both the load and PV inverter model can be implemented using controlled current sources, so for simplicity a combined block representing both single-phase PV inverter and load is implemented. The synchronized injection currents are calculated based on the following **Equations(12)** and **(13):**

$$S_p = V_{rms} * I_{rms}^{*} \rightarrow I_{rms} = conjugate(\frac{S_p}{V_{rms}}) \quad (12)$$

$$P_p = Re\{S_p\};\ Q_p = Im\{S_p\} \quad (13)$$

Where, S_p, V_{rms} and I_{rms} represents per phase complex power, nominal RMS voltage and RMS current. To have the block operate in both feed-in and consumption mode, the value of the power plays a vital role. The resultant power values from PV profile and load are treated mathematically in the following manner as shown in **Equation(14),** before evaluating the final injection currents.

$$P_R = P_{load} - P_{inv}\ ;\ Q_r = Q_{load} - Q_{inv} \quad (14)$$

Where P_r and Q_r represents the active and reactive powers based on which the current controlled input signals are evaluated to generate injection currents at the grid connection point. If $P_r > 0$ it acts as a load for the grid , if $P_r < 0$ it acts as a feed-in source to the grid, if $P_r = 0$ it would assert that at that particular instant the load demand is fulfilled by the PV so no power is drawn or fed to the grid.

The P_{load} and Q_{load} are defined by the load profile time series whereas P_{inv} is defined by the feed-in profile time series. However, the Q_{inv} is the input from the Q-management block explained in the following section. Another reason to have such a hybrid load block in the model is that, the HUT in

PHIL setup can be operated in regenerative mode / feeding mode dynamically as explained in **section 2.3.1.2**. So, this block can also serve to test the dynamic response of HUT during real-time PHIL simulation. The **Figure 3.7** below shows the hybrid load block implemented in Simulink. It is the detailed expansion of the sub-system Load phase at Bus H102 shown in **Figure 3.3.**

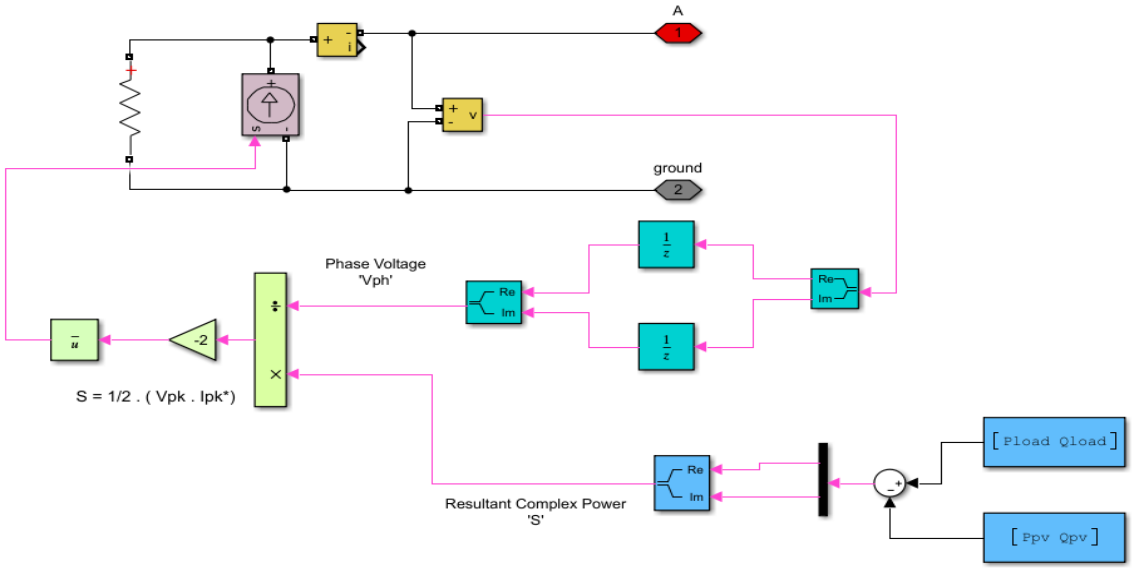


Figure 3.7 Hybrid load block developed for each phase in Simulink.

3.3 Reactive Power Management and Control

The reactive power controls to be implemented in real-time are governed via the Q-Management block. The structure of the complete inverter's Q-management is illustrated in **Figure 3.8.** The management block is implemented in the phasor framework to check its response while executing the dynamic time series power flow analysis in phasor domain. The main function of this block is to provide the reactive power set-points depending upon the chosen smart inverter controls. The main input to the block is per unit phase voltage V_{ph} at the bus terminals.

The unit delays are introduced in the block for different measurements. Initially the phase voltage is measured and passed on to the smart inverter control block with a time delay (T_v) of 100 ms. The contemporary inverters use five grid periods to calculate the moving RMS value of the voltage [27] based on which the reactive power is evaluated in case of voltage dependent reactive / active power injection. As the system frequency is 50 Hz, this adds up to a time constant of 100 ms for five grid periods. So, the moving mean for phase voltage is calculated over a time period of 100 ms. In this study, only in volt-var strategy the reactive power injection depends upon the voltage.

Similarly, the resultant active and reactive power evaluated by the smart inverter block are injected with a time delays of (T_p=0.1 s and T_q=0.1 s). Typical values for these time constants are in the range of few seconds to minutes and can be configured via the graphical interface of state-of-the art inverter [27]. The time delays specified basically determines how fast the power output of an inverter will change based on the change in phase voltage [27], power feed-in etc. A low time-delay is opted to observe the fast-dynamic changes with respect to varying power set-points from the modelled hybrid load block.

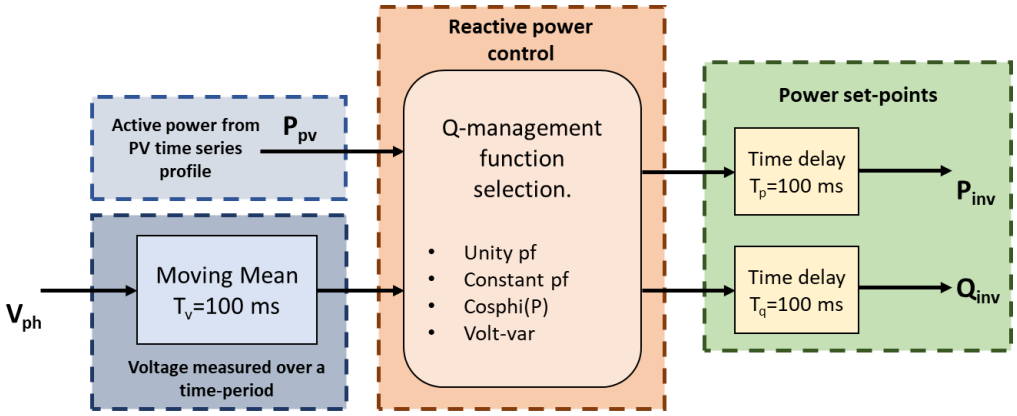


Figure 3.8 Process flow of Q-management (smart inverter control) modelled in Simulink.

The smart inverter block basically enables to choose the control based on the state-of the art techniques being implemented in inverters as discussed in **section 2.2.3**. It is modelled as a variant sub-system in Simulink with two inputs (PV power and phase voltage at the bus terminals) as shown above in **Figure 3.8**. Different controls are implemented inside the block as MATLAB scripted functions. Brief detail into every function is defined below:

3.3.1 Unity Power Factor

The first one is a very simple unity power factor function. The reactive power output from this block is 0, whereas the active power is passed to the output as it is.

3.3.2 Constant Power Factor

The second function implements the constant power factor control. This means that the reactive power output from this function will be a constant value based on the power factor and active power input. The power factor chosen is 0.9 lagging, although as discussed **in Table 1** for PV system ratings between 3.5 to 13.8 kVA the pf should be 0.95 but in order to observe some dynamic changes in voltage and to have comparatively high amount of reactive power the pf of 0.9 lagging / leading in general is used for Q-control and voltage regulation. In this function the reactive power output is calculated by using **Equation(9).**

The PV power profiles integrated in this study are assumed to be at unity pf, so for strategies other that the unity pf the active power output will also be reduced based on the operating pf. This is done to model the inverter's response close to real life operations as the capacity of an inverter is limited by the apparent power.

3.3.3 Cosϕ(P)

In this function the cosφ(P) characteristics are implemented as shown in the **Figure 2.8**. When the ratio of feed-in ($P_{available}/P_{max}$) is up to 0.5, no reactive power will be injected i.e. the pf =1. Above 0.5, Q will vary as a function of pf as per VDE-AR-N 4105 regulations[4]. The varying pf at a particular power feed-in is determined by the slope equation. The same **Equation(9),** is used to evaluate the reactive power based on the active power and the pf.

3.3.4 Volt-Var Q(U)

Finally, the last control is volt-var which injects voltage dependent reactive power. For a low-voltage grid the allowed voltage regulations are within the range of ± 10 % of the nominal voltage based on the EN-50160 standard [40]. This implicates that usually the region between (0.9 – 1.0 pu) is a dead-

band with no reactive power output, but the Q(U) characterization depends on case to case. However, in this case the voltage variations are not very high considering the non-complex structure of MONA networks therefore the voltage dead-band is reduced to (0.98 – 1.02 pu). Below and above these values the reactive power will be available from inverters in over / under excitation mode, respectively.

Concerning the Q_{max} value, the limits are restricted to pf = 0.9 depicting controlled reactive power injection from the inverter. In uncontrolled mode, the reactive power provided by the inverters could vary depending upon the active power. As from **Equation(10),** the lower the active power gets; the high reactive power is available from the inverter. The implemented volt-var characteristic curve is illustrated in **Figure 2.8**. Q-values at a particular voltage are calculated mathematically inside the functions using the defined set of equations shown in **Figure 2.9.**

3.4 Test and Validation of Simulink Model

To test whether the developed grid model in Simulink is functioning properly specially with the hybrid load block and Q-management functions, the validation of the same needs to be performed. The same model is tested in a different environment and the results are compared with the simulation studies performed in Simulink phasor domain. OpenDSS – an open source power distribution system simulator is chosen to perform the validation. Unlike Simulink, a distribution network is specified in a scripted form in OpenDSS platform. Each of the elements source, loads, transformer, lines etc. are specified via lines of codes with complete specifications.

For validation purposes, MONA-8002 network is implemented in OpenDSS, most of the model is already scripted as obtained from the MONA project source [37]. The remaining part was to add the loads, specify the load profiles and incase of PV specify the PV system, feed-in profile, and desired inverter control. Excerpts of the MONA-8002 OpenDSS script is provided in the **Appendix A.2**. The following scenarios for MONA-8002 network validation are executed in Simulink and OpenDSS.

Table 4. Scenarios tested for model validation.

<table>
<tr><th>Scenarios</th><th>Load / PV Profiles</th><th>Simulation Time</th><th>Sample-Time</th><th>Observation</th></tr>
<tr><td colspan="5">Conventional Uni-Directional Grid</td></tr>
<tr><td>No-Feed in. Only Loads connected at the Buses.</td><td>Unbalanced SP household profiles with a temporal resolution of 1s.</td><td>One Day ~ 86400 seconds</td><td>Simulink - 100 ms / - OpenDSS ~ Computing solution at step-size of 1s</td><td>Voltage profiles at the load bus</td></tr>
<tr><td colspan="5">PV Feed-in at Bus H102 and Inverter Controls</td></tr>
<tr><td>Feed-in at unity pf</td><td rowspan="2">SP PV profiles with a temporal resolution of 1s.</td><td rowspan="2">One Day ~ 86400 seconds</td><td rowspan="2">Simulink - 100 ms / - OpenDSS ~ Computing solution at step-size of 1s</td><td>Voltage profiles at the PCC.</td></tr>
<tr><td>Feed-in with Volt-Var Q(U) control</td><td>Voltage and reactive power profiles at the PCC.</td></tr>
</table>

Brief description into each scenario and analysis of the results is defined in the following section.

3.4.1 Scenario – 1. Only Loads Connected

The structure of the 8002 network is already shown in **Figure 3.1**. SP loads are connected at both the buses with profiles of 1s in both the platforms. In Simulink, the SP dynamic load block is connected at the buses while in OpenDSS the loads are defined in a script with a customized load profile. The results of this scenario are illustrated below:

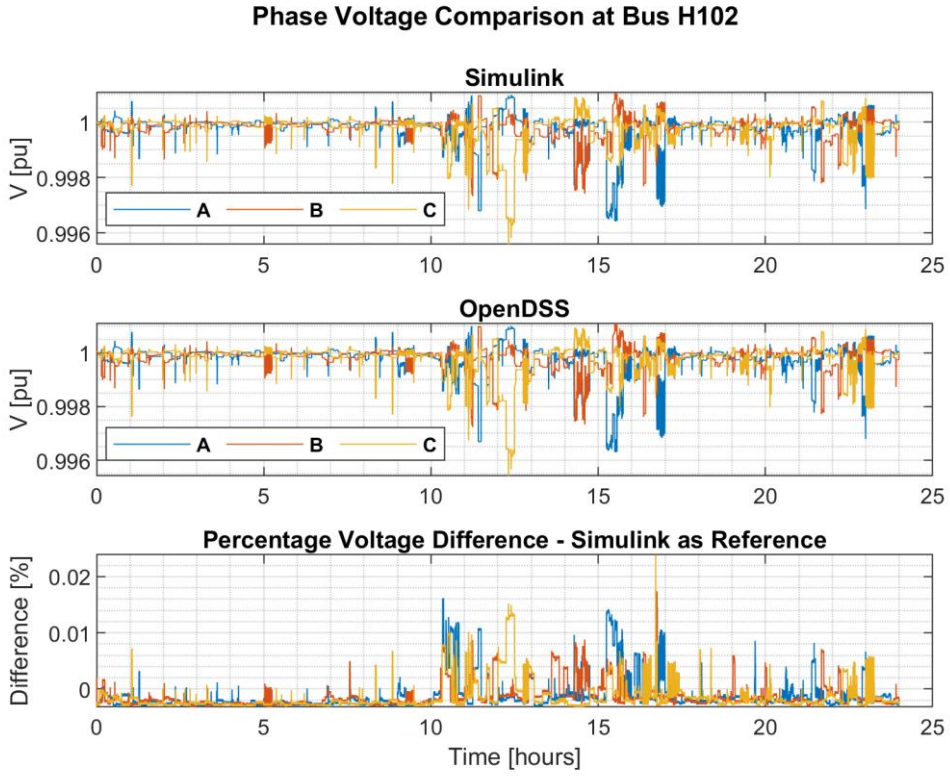


Figure 3.9 Phase voltage comparison between Simulink and OpenDSS (No Feed-in).

The first two subplots represent the phase voltage (A, B, C) profiles from both the platforms. It can be seen that in case of only loads, the network voltages are quite stable and fluctuates around 1 pu. Concerning the comparison, the trend is the same from Simulink results as obtained from OpenDSS. To visualize the difference between the two, a third subplot is added representing the percentage difference with Simulink as reference. The difference is very low which indicates the voltages are merely the same. The highest difference is observed in phase C voltage where the voltage in Simulink is 0.024% more than the OpenDSS value. To put it statistically, if the OpenDSS value at this particular instant is assumed to be 230 V than from Simulink it is around 230.05 V.

From this scenario the response of single-phase dynamic load block of Simulink as a current-controlled source is tested and validated in operation with the LV grid. It is observed that the voltage values show a very insignificant difference.

3.4.2 Scenario – 2. Addition of Feed-In at Bus-H102 at Unity PF

The PV feed-in is now introduced in the grid at the second load bus. In OpenDSS a new SP PV system is defined and interconnected at each phase of H102, customized feed-in profiles are defined as load shapes to be followed by the PV system. From the first scenario it has been observed that the voltages are almost around 1 pu, so for validation the normalized PV profile with a peak power of 15 kW_p is used to observe significant change in voltages. The PV profile used is shown in the **Figure 3.10** below.

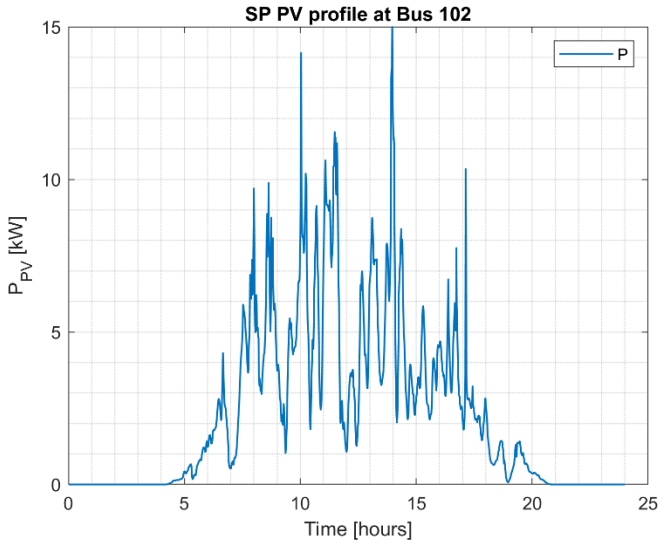


Figure 3.10 PV profile integrated at Bus 102.

The PV inverter is operating at unity pf in this scenario. In Simulink, the hybrid load block is connected at H102 while the inverter control in Q-management block is set to unity pf. The results are shown below:

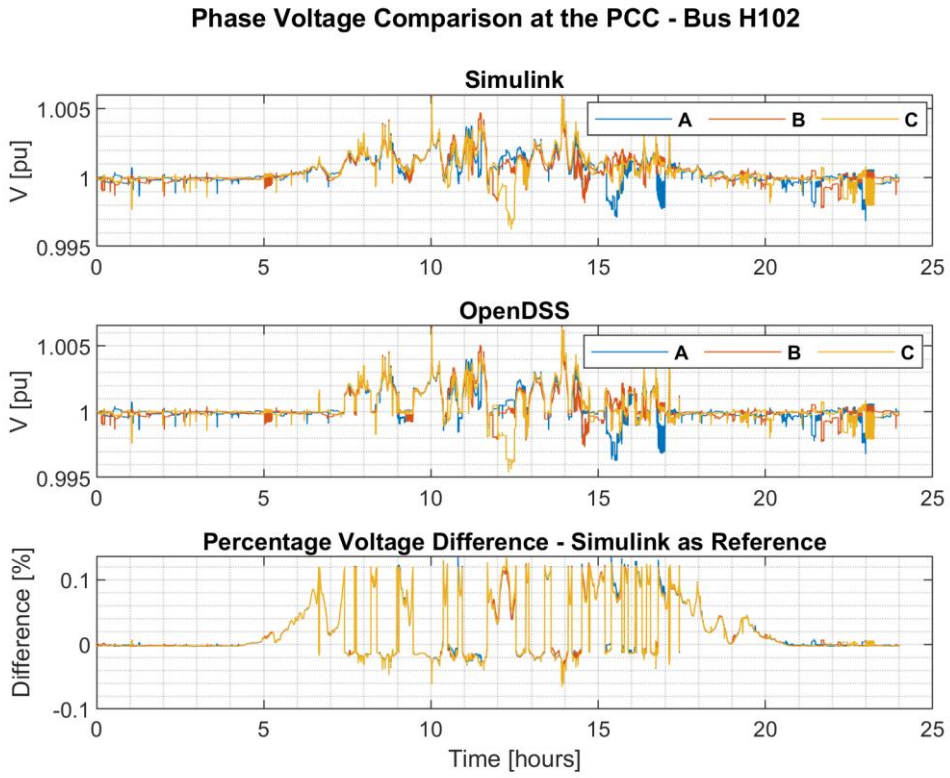


Figure 3.11 Phase voltages comparison between Simulink and OpenDSS (PV at unity pf).

The effects of feed-in can be observed as the voltage rises from the nominal value during midday with a peak phase C voltage of 1.005 pu at maximum feed-in. The voltage trend exhibited by Simulink is similar to that of OpenDSS. From the third subplot, the difference can be visualized. During the start and towards the end of the day, the difference is very low. However, during midday when power is

injected by PV, the difference is a bit higher. The highest difference of 0.12 % is observed in voltage values. Again, putting it statistically this will render a voltage of 230.2 V from Simulink when it is 230 V from OpenDSS. At some instants, the percentage difference is negative depicting that the Simulink has a low value compared to OpenDSS. The difference is very low though around -0.06%.

The overall difference is still very minimal. Compared to the first scenario, it is 0.15 V more. This could probably due to the fact that the inverter / load is modelled as a simple current-controlled source in Simulink without going into many details. Whereas, in OpenDSS two elements are used separately one as a load and one as PV system. Also, the timestep could be a reason as OpenDSS computes solution at each timestep in this case 1s whereas in Simulink the sample time is 0.1s. The profiles are of 1s resolution, so it interpolates the values at each sample-time in Simulink. This adds more dynamics to be observed at millisecond level. Nevertheless, the response of the Simulink model is fairly well to conduct power flow analysis as the difference obtained is very low. From this scenario the response of hybrid load block of Simulink acting both as a source and a sink is tested and validated in operation with the LV grid.

3.4.3 Scenario-3. Inverter Control Set to Volt-Var

As volt-var is dependent on the voltage, the Q set-points changes dynamically during the time series phasor simulation. Therefore, this control is tested for validation. In OpenDSS, under this control option at any instant the total available reactive power from the inverter is injected based on the active power feed-in. However, in Simulink the volt-var control is operating in a controlled manner with Q_{max} limited to 0.9 pf (leading/lagging). For this reason, the Q-output implemented in OpenDSS is limited to 44% of the rated apparent power i.e. at a pf of 0.9, as illustrated in the **Figure 2.7**. The Q(U) characteristic curve implemented for this particular scenario is shown in the **Figure 3.12** below.

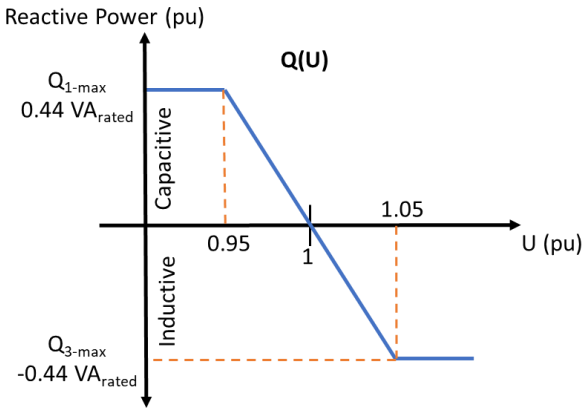


Figure 3.12 Q(U) characteristic curve.

Thus, when the per unit voltage is 1 no reactive power is available other than that there will always be a reactive power from the inverter side. For this scenario, the comparison is made not only based on the voltage but also on reactive power. The results obtained are shown below. Firstly, the phase voltages:

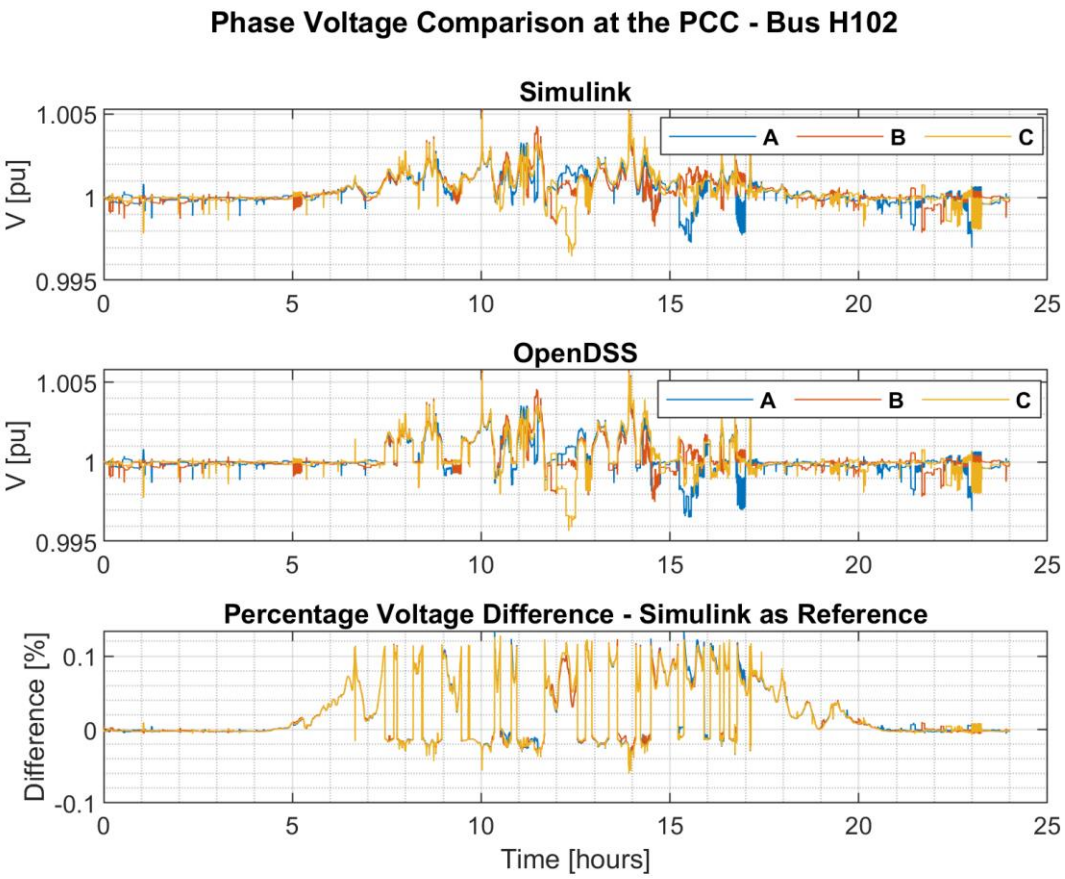


Figure 3.13 Phase voltages comparison between Simulink and OpenDSS (PV with volt-var control).

With the inverter control, the voltage values did change but not very significantly as the network is quite stable. The maximum reactive power would not be injected at any instant from the inverter as the voltages are well within 0.95 – 1.05 pu. The idea behind is to just test the response of inverter's reactive power and compare the values.

Similar to the previous scenario, the voltage difference is the same in this scenario. Therefore, in terms of voltage the Simulink model exhibits satisfactory performance under Q-management. Another interesting parameter to observe in this scenario is the reactive power at the PCC i.e. Bus 102. The **Figure 3.14** below shows the results.

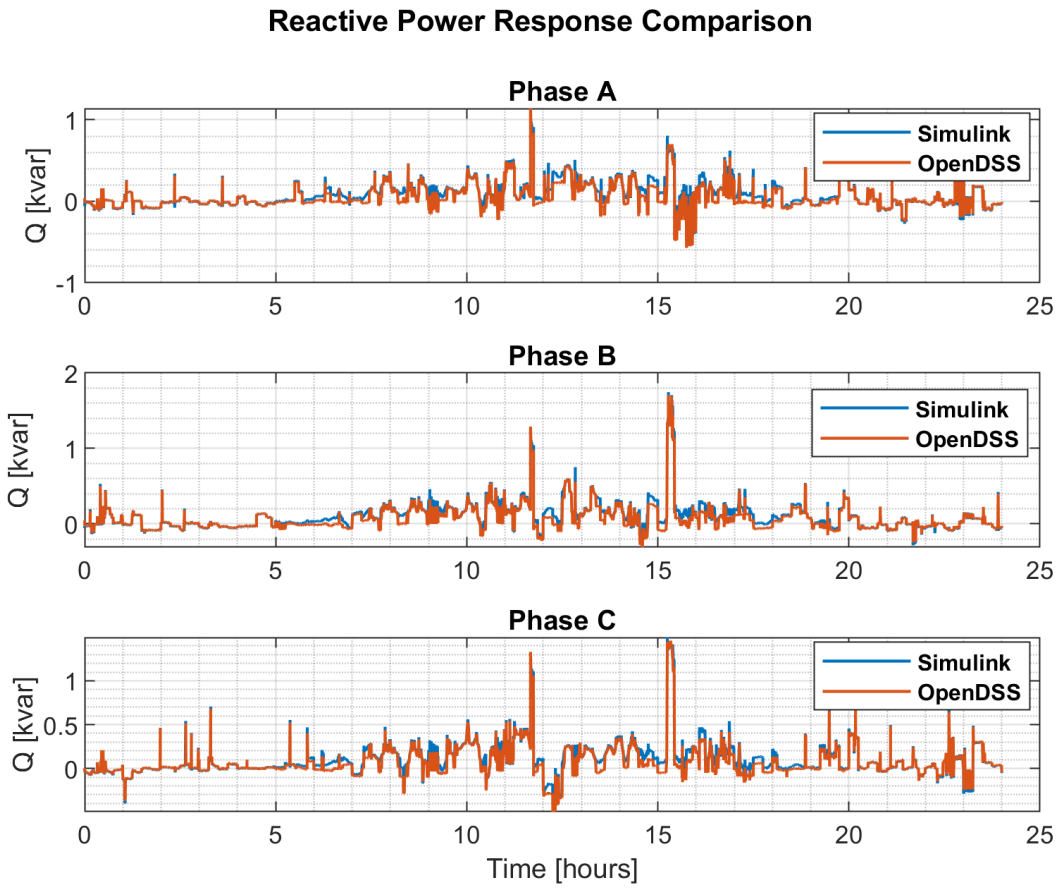


Figure 3.14 Reactive power at Bus 102.

The reactive power response from both the platforms is observed under volt-var control. As seen from the plot above, for all the phases the reactive power response from Simulink almost overlaps the output from OpenDSS. A minor difference is observed at some instants. In general, it is similar depicting the operational fidelity of Q-management function block developed in Simulink. The dynamic Q response from the Q-management block developed in Simulink is tested and validated through this scenario.

Overall the validation results show that the SP dynamic load block, hybrid load block and the Q-management functions developed in Simulink environment are operating in synchronization with the LV grid and the Q- management is also contributing towards voltage compensation to some extent based on the dynamics of the grid. All inverter controls are not tested as volt-var is the one with the most dynamic changes. It is assumed that better performance of the tested control ascertains the Q-management block functionality in general. The validation is performed to grasp the overview of the Simulink model. Apparently, there are minor differences because of the fact that the Simulink model blocks does not involve too much complexity. This is just to make sure that the variations are not very significant and developed model in Simulink phasor framework is suitable to conduct the power flow analysis.

3.5 MONA-8008 Dynamic Time-Series Power Flow Analysis (Phasor)

After validation of the Simulink model, the same approach is scaled-up to implement a comparatively complex MONA-8008 network. Likewise, the simulation studies are performed in the phasor

framework i.e. the solution is computed at the system's fundamental frequency. Although for real-time PHIL simulation the hybrid simulation interface is used as explained in the next **section 4,** but phasor analysis is done to observe the holistic overview and the dynamics of the network under multiple Q-controls and excess feed-in at the load buses. Effects on voltage variation at the buses due to controlled feed-in are also observed. Similar scenarios as observed during the validation are performed with additional Q-control functions and some minor differences as outlined in the **Table 5** below.

Table 5. Scenarios evaluated with MONA-8008 network.

Scenarios	Load / PV Profiles	Simulation Time	Sample-Time
Conventional Uni-Directional Grid			
No-Feed in. Only Loads connected at the Buses.	Balanced SP household profiles with a temporal resolution of 1min.	One Day ~ 1440 mins.	100ms
PV Feed-in at All Buses			
Feed-in with unity pf	Balanced SP PV profiles with a temporal resolution of 1min.	One Day ~ 1440 mins.	100ms
Inverter Controls – Only applied at Bus-H108			
Constant pf	Balanced SP PV profiles with a temporal resolution of 1min.	One Day ~ 1440 mins.	100ms
Cosφ (P)			
Volt-Var Q(U)			

As the PV / load profiles are with a resolution of 1min, when the model is simulated at a sample time of 100ms the values in between the timesteps are linearly interpolated. For complete PV feed-in analysis in the 2nd scenario, the hybrid load block is connected at each of the buses depicting feed-in at unity pf. The smart Q-control functions are only implemented at bus H108 which is the farthest node from the transformer supply. The following single-line diagram of MONA-8008 illustrates the idea after integration of feed-in units.

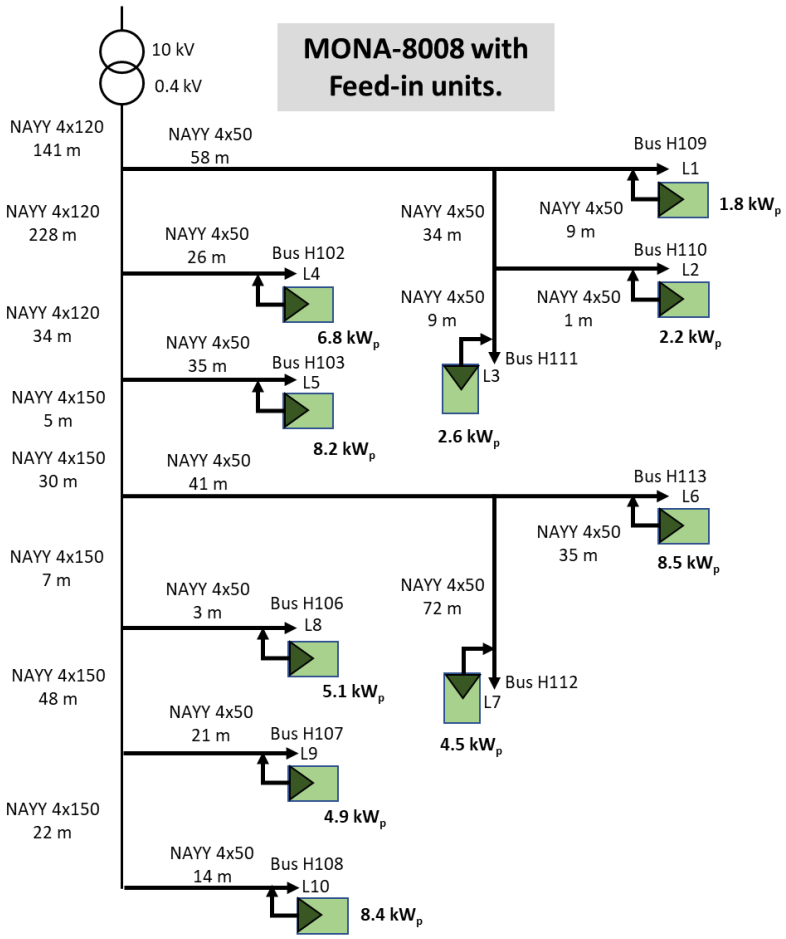


Figure 3.15 MONA-8008 network with feed-in per phase capacity.

For the inverter controls, the characteristics curves used for cosφ(P) and volt-var Q(U) are the same as shown in the **Figure 2.8**. Similarly, the load profiles used in the analysis are defined in **Table 3.** Accumulated results from all the scenarios are discussed in detail in the following section.

3.6 Desktop Simulation Results of MONA-8008

The results from the simulation are not discussed scenario wise rather a general overview is presented covering all the scenarios. To analyze the power flow conducted in the phasor domain, the following variables are focused and explained in this section.

- Load duration curve.
- Voltage color map.
- Reactive power flow and voltage with all Q- controls.
- Box plots for voltages with different controls.
- Power flow at the LV grid transformer.

3.6.1 Load Duration Curve

Firstly, the load duration curve is shown to observe the extent of reverse power flow and how often the LV grid experiences the power feed-in.

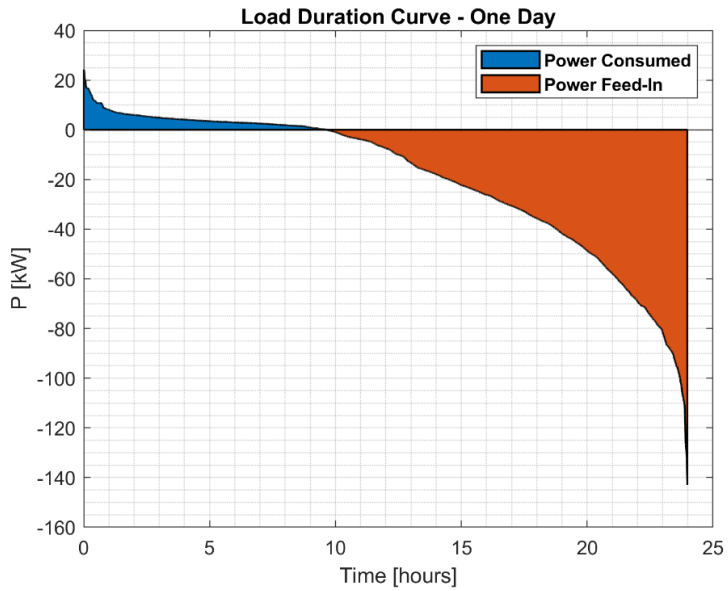


Figure 3.16 Load duration curve of the LV grid.

The load duration curve is plotted for the 2nd scenario when there is a feed-in at all the buses with unity pf. From the **Figure 3.16** above, it is evident that there is excessive feed-in with a maximum of [approx. 145 kW] surpassing five times the maximum power demand of [approx. 25 kW]. The curve is plotted for one complete day and the reverse power flow persists for more than half of the time during the whole day. With such a significant feed-in the nominal voltages are expected to alleviate expressively from the nominal values.

3.6.2 Color Map for Voltages

To capture a one frame overall view of the network voltages, the color map is plotted having all the bus voltages for each phase. The network is integrated with balanced load and PV profiles, thus the voltage at each phase of a particular bus would be the same.

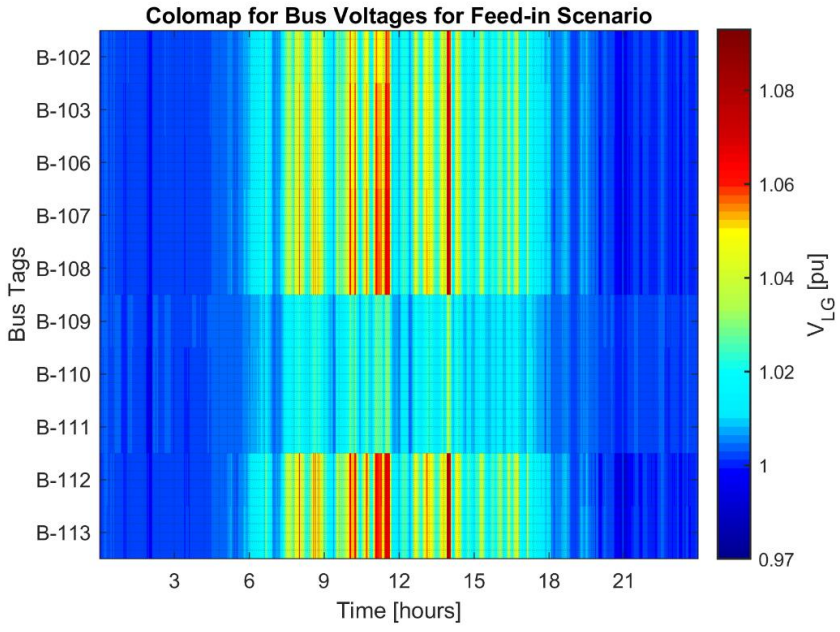


Figure 3.17 Color map for phase voltages at each bus.

In **Figure 3.17** above, the y-axis indicates the bus tags with all three phase voltages plotted horizontally against time. The scale is presented on the right side of the plot with pu values for respective color regions. The color map explicitly illustrates the voltage fluctuations during mid-day when feed-in is maximum. The yellow and red color spots indicate higher voltages than nominal starting from 1.04 pu and beyond. The start and end of the day have voltage levels around the standard 1 pu. The highest voltage level almost reaches to 1.08 pu at all the buses except 109,110 and 111 as at these buses the peak feed-in is very less compared to other buses, refer **Table 3.**

3.6.3 Voltage Boxplots with Different Q-Controls.

After analyzing the network under complete feed-in, the next step is to observe the effect of developed Q-management functions. All the Q-controls are tested at Bus 108, to grasp the complete picture of the effects of different controls on the bus voltage the bar chart is plotted as shown in the **Figure 3.18** below.

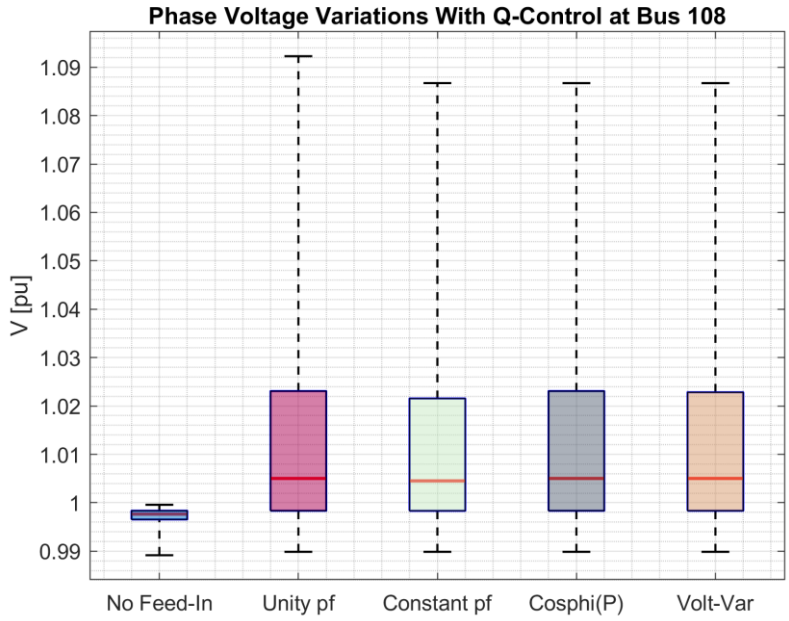


Figure 3.18 Voltage boxplots for all Q-controls.

Starting from the conventional scenario, the voltage bar chart is illustrated separately for each feed-in scenario with respective Q-control. Under no feed-in, the voltage at the bus seems to be quite stable between 0.99 – 1 pu. A huge spike is observed in complete uncontrolled feed-in scenario at unity pf with maximum voltage of up to 1.092 pu. For all the feed-in scenarios, it can be observed that 25 % of the observations are greater than 1.02 pu, indicating the voltages during feed-in time of the day. The centered value i.e. the median is however 1.005 pu. With different Q-controls it can be seen that the maximum voltage level has dropped to around 1.085 pu from 1.092 pu. Almost for all the Q-controls the maximum voltage threshold is the same, due to the fact that all the controls has a constraint of 0.9 pf to inject the reactive power as described in **section 3.3**. If different pf settings are opted for each control, the voltage variation would also be different in each scenario.

Furthermore, the minimum voltage value is also the same for each control. In volt-var the reactive power flows in both ways in under-excited and over-excited region. The threshold to operate in over-excited region is below 0.98 pu refer Q(U) curve in **Figure 2.8**. But in this case, it is apparent from the

conventional power flow circumstances that the lowest voltage is around 0.99 pu and after feed-in it is further pushed up slightly. So, in principle when volt-var control was active, it was always operating in under-excited region i.e. inductive reactive power. Otherwise, the lowest voltage value would also have been affected in volt-var control scenario and the minimum voltage threshold would be different.

The **Table 6** below specifies the voltage statistics at bus 108 for each of the respective scenarios shown in the bar chart above in **Figure 3.18.**

Table 6. Summarized voltage statistics at Bus 108 under each scenario.

	No Feed-in	Unity_pf	Constant_pf	Cosφ_P	Volt_Var
Max Voltage [pu]	1	1.092	1.087	1.087	1.087
Min Voltage [pu]	0.989	0.99	0.99	0.99	0.99

From the **Table 6** above, it can be established quantitatively that a decrease of 0.05 pu equivalent to 1.15 V is experienced after applying the controlled feed-in strategies.

3.6.4 Inverters' Reactive Power Response and Phase Voltage Under all Q- controls.

Now that the effectiveness of the smart inverter controls is analyzed, a more detailed insight into each control would be to observe the reactive power response from the Q-management block with varying voltage. The plots below represent the same.

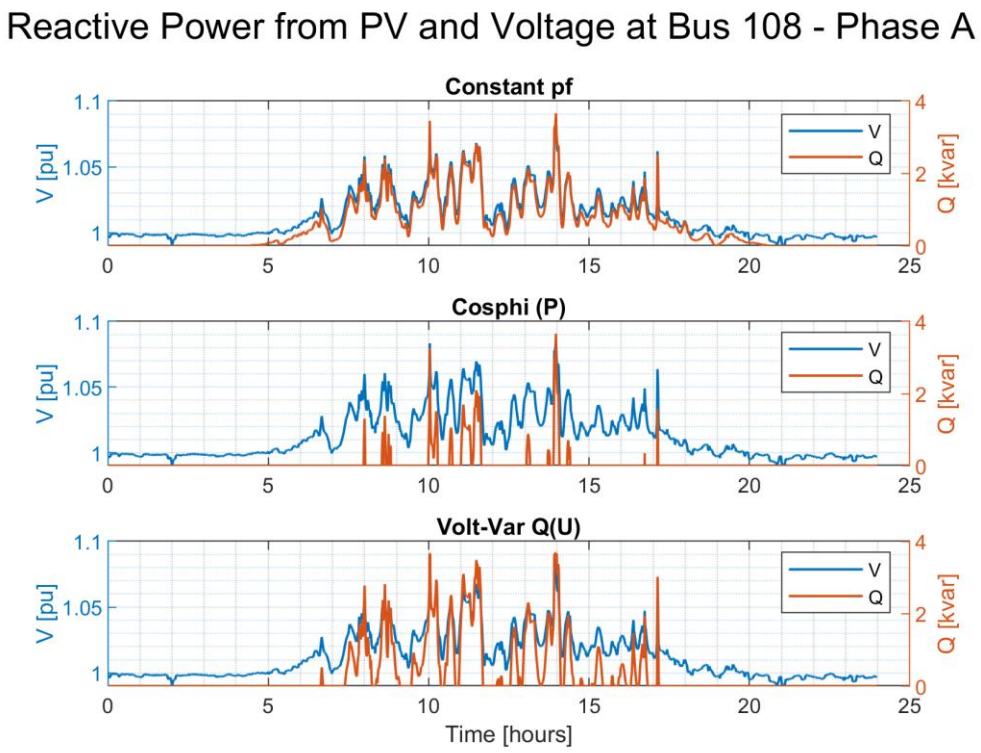


Figure 3.19 Reactive power response for reach Q-control.

The first sub-plot in **Figure 3.19** above shows the phase voltage(blue) and reactive power(orange) profile under constant pf control. The modelled inverter is supposed to operate in under-excited mode in this particular control with constant inductive reactive power throughout based on the active power input. During start and towards the end of the day there is no reactive power as active power feed-in is zero. The reactive power follows the trend of the voltage as it is also directly dependent on the active power feed-in trend.

Contrary, to the constant pf in the second sub-plot it can be observed that the reactive power response from the inverter is not continuous. As it is supposed to contribute only when the active power feed-in is more than 50% of the maximum feed-in. A high voltage than the nominal indicates high feed-in and it can be seen that at those time instants the modelled inverter is operating in under-excited mode absorbing reactive power. At most of the instants during the day the reactive power response is idle because of low feed-in ($P_{available}/P_{max} \leq 0.5$).

Lastly, the third sub-plot is for the volt-var control. There is no capacitive reactive power at all**.** However, when the voltage is beyond 1.02 pu the inductive reactive power is present from the modelled Q-management block and being absorbed by the modelled inverter. These would be the reactive power responses required by the current controlled amplifier (HUT) during PHIL test under Q-management application in real-time

3.6.5 Power flow at the LV grid transformer

Finally, the power flow from the grid's transformer LV side is plotted to observe both the active and reactive power fluctuations of the grid. The graph below shows the result.

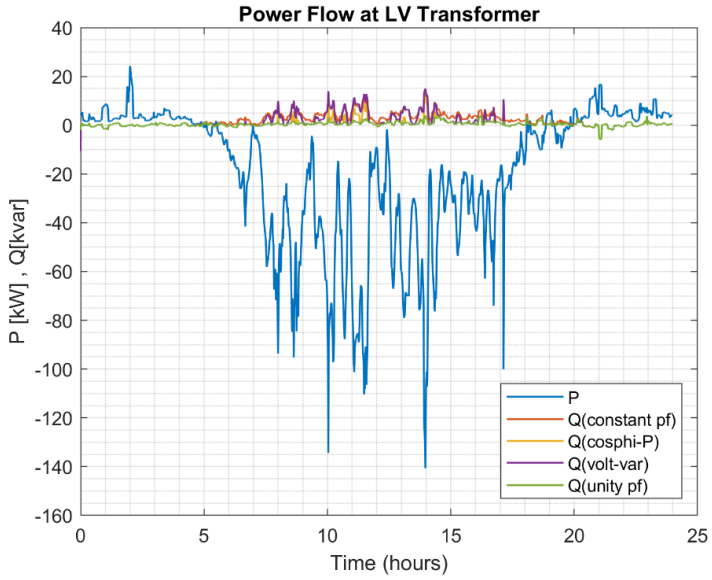


Figure 3.20 Active and reactive power flow.

The **Figure 3.20** above summarizes all the scenarios in terms of grid power flow. Complete reverse power flow is experienced by the grid transformer from 05:00 to 19:00 hr. Additionally, during the same time window a high inductive load demand is being observed by the grid in case of constant pf (orange plot) and volt-var (purple plot) scenario. Whereas, for unity pf the nominal reactive power as that of the connected loads is being drawn from the grid shown by the green plot.

3.7 Summary

The complete development of the simulation testbed is explained in this chapter. The components utilized to build the grid model are described. The robust Q-management functions implemented as a top layer for the hybrid load block are also explained. The validation of the model and Q-management block is performed by comparing the results of the defined scenarios with another open source power distribution system simulator. The results from the offline simulation are analyzed and effectiveness of Q-management is illustrated. Overall, the grid model seems suitable to conduct the power flow analysis, observe effects of feed-in and additionally the implemented Q-controls strive to contribute towards voltage regulation.

4 Simulink-MATLAB As Hybrid Simulation Interface

To develop the hybrid simulation interface, the important aspect is the equivalent sub-systems and the interface bus at which the exchange of data takes place. The approach used for developing the hybrid simulation model of both the grid networks considered in this study is the same, the only difference is the interface bus. The selection of the interface bus usually depends on which part of the network requires detailed analysis. However, as already stated that the PV inverter is not modelled in detail in this work so the selection of interface bus is done based on the fact that on which bus the hybrid load block is connected and for which bus the voltages will be emulated in RT PHIL simulation. In case of MONA-8008, it is bus H108 at which the network partition is performed and for MONA-8002 it is bus H102.

4.1 Equivalent Sub-System Representation

After partition, the model is split into two parts one simulated in the phasor and the other in EMT domain discretized at a sample-time of 100 µs. The interface bus is connected to an equivalent representation of both the sub-systems in respective domains. The phasor sub-system is represented via a Thevenin equivalent circuit i.e. a controlled voltage source and an impedance in the discrete domain.

The corresponding voltage (magnitude and phase) at bus H108 is extracted from the phasor domain. The values are transformed into three time-varying waveforms in discrete domain at the fundamental frequency using the following **Equation(15)**.

$$V = V_m * sin(2\pi f t + \theta_p) \tag{15}$$

Where, V_m and Θ_p is the magnitude and angle of the voltage phasors obtained from the phasor domain. The voltage waveforms for each phase are fed to the controlled voltage sources after which the sinusoidal voltage is generated. To evaluate the Thevenin equivalent impedance of the phasor model the Impedance Measurement block is used. The block measures the impedance between the two phases as a function of frequency. The block is connected between the two phases at bus H108 to evaluate the total impedance of the network as seen upstream from the bus.

The impedance measurement option from the powergui block in Simulink can be used to generate the magnitude and angle of the impedance. For a three-phase circuit, to acquire the positive sequence impedance the multiplication factor of (½) is to be used to rescale the measured impedance [41]. As measuring the impedance between the two phases would give two-times of the positive sequence impedance. The real part of the impedance represents the value of the resistance whereas for the reactive part the corresponding value of the inductor is evaluated by using the following **Equation (16)**.

$$Z_{pm} = Z_r + jZ_L \rightarrow R = \frac{1}{2} * Re\{Z_{pm}\}; L = \frac{1}{2} * Im\{Z_{pm}\} \rightarrow \frac{1}{2} * \frac{Z_l}{2 * \pi * 50} \tag{16}$$

The equivalent impedance is only measured once and assumed constant as no modifications are made in the network configuration. The following **Figure 4.1** represents the equivalent phasor sub-system representation in discrete domain developed in Simulink.

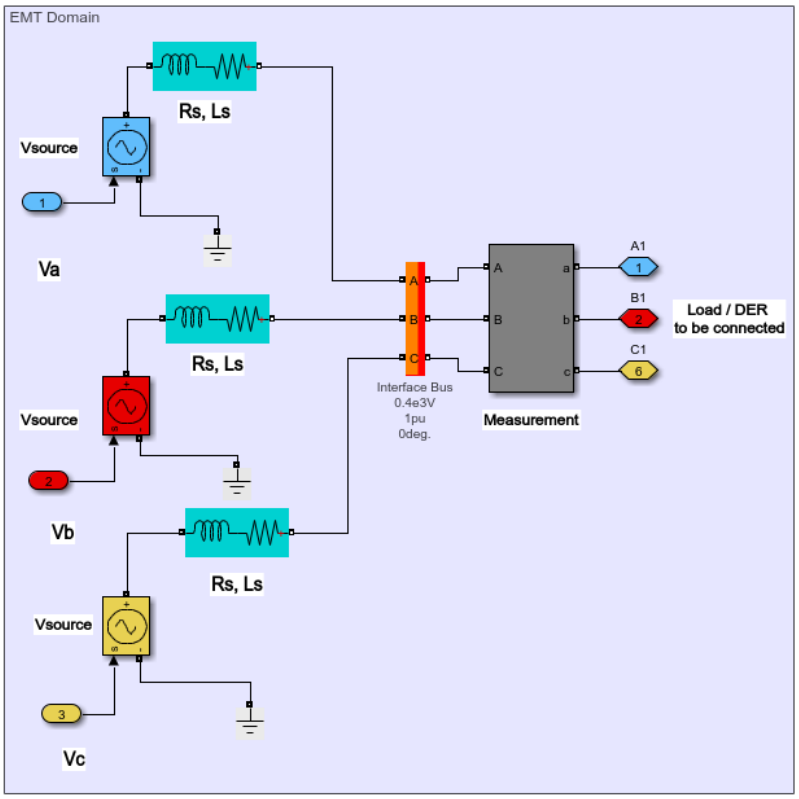


Figure 4.1 Phasor network representation using Thevenin equivalent in discrete domain.

Similarly, the discrete system is represented in the phasor domain via a Norton equivalent circuit with a controlled-current source and a parallel impedance. Phasor values at the fundamental frequency of the current waveforms from the discrete domain are required to be fed back to the phasor domain. To convert the instantaneous waveforms into phasors the Fourier Transform block in Simulink is used which extracts the fundamental magnitude and angle of the respective phase currents to be fed as a control signal to the controlled-current sources in phasor domain. The respective currents are then generated by the current sources modelled in phasor domain. A high value impedance is connected in parallel with the controlled-current sources in phasor domain. The following **Figure 4.2** represents the equivalent representation of discrete sub-system in phasor domain developed in Simulink.

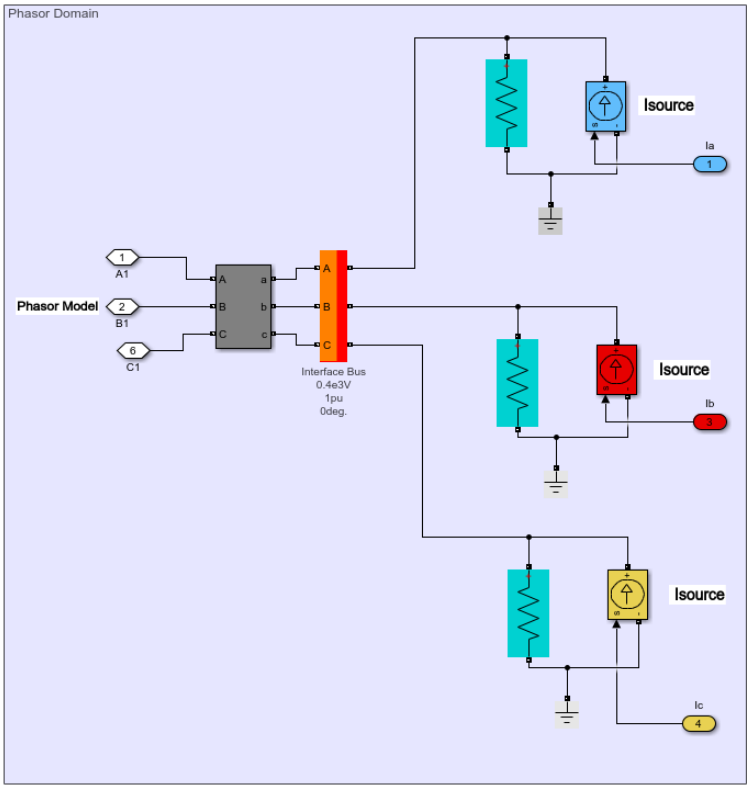


Figure 4.2 Discrete system representation using Norton equivalent in phasor domain.

4.2 Complete Hybrid Simulation Interface

The two sub-systems are interconnected with each other in a single model. Two different powergui blocks are placed in each sub-system. The phasor domain has a phasor solver at the fundamental frequency of 50 Hz while in discrete domain the solver is set with a sample time of 100 µs. Both of the sub-systems are operating simultaneously following a parallel protocol. In a nutshell, the instantaneous phasor values are transmitted to the discrete domain to be converted to waveforms. Likewise, the phasor values are extracted from waveforms in discrete domain and transmitted to phasor domain with a step time-delay to represent the total power being consumed / injected in the network at each time instant. The whole data exchange takes place at the interface bus H108. The complete hybrid simulation interface of MONA-8008 network with sub-systems is illustrated in the **Figure 4.3** below.

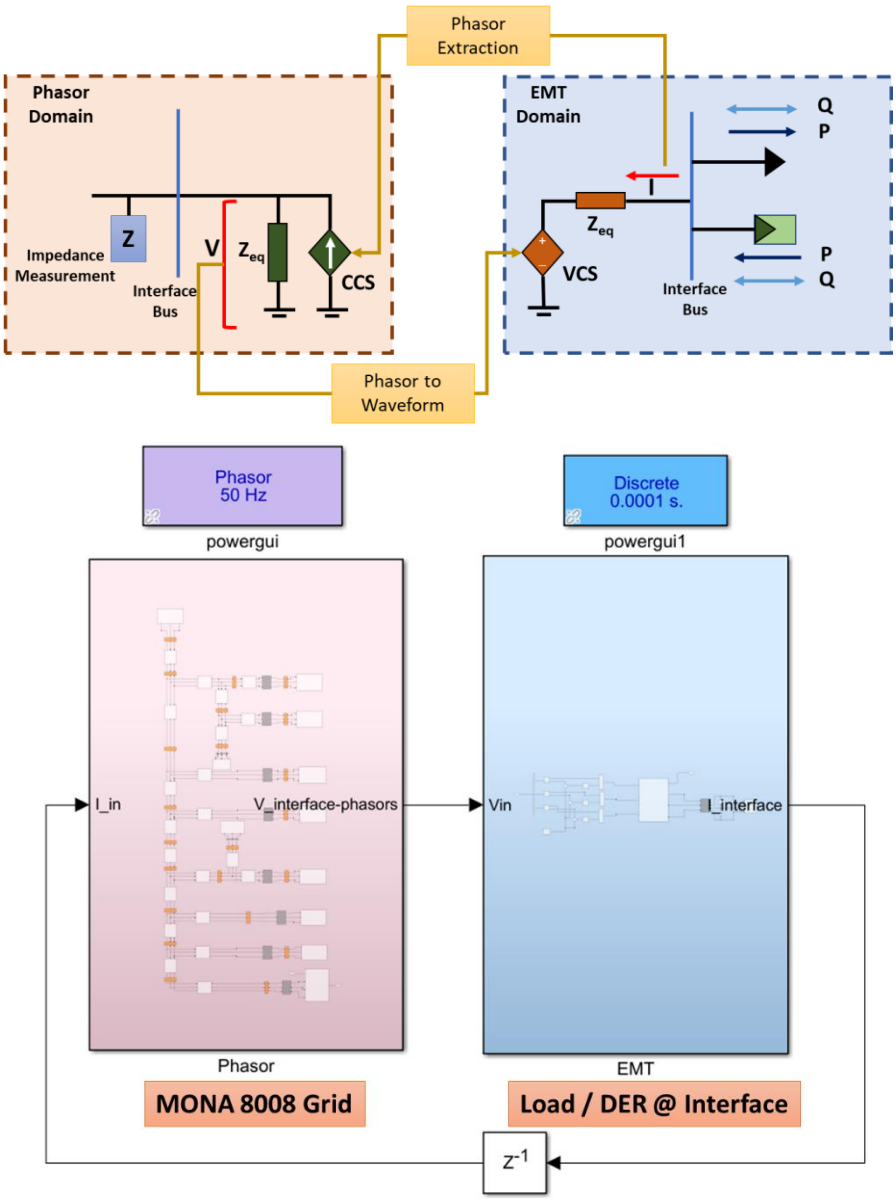


Figure 4.3 Hybrid simulation data flow and interface in Simulink.

The top part of the **Figure 4.3** represents the exchange of variables at the interface bus between the two sub-systems. The bottom part of the **Figure 4.3** illustrates the hybrid model developed in Simulink. The variable exchange is shown by black arrows. The process of phasor extraction and conversion to waveform is performed inside the sub-systems following the method as described in **section 2.1.3**.

4.3 Scenarios Implementation

To observe the functioning of MONA-8008 hybrid simulation model, the following scenarios are implemented as outlined in **Table 7** below.

Table 7. Scenarios to Observe Functioning of Hybrid Simulation Model.

Scenarios	Load / PV Profiles	Interface Bus	Simulation Time	Phasor / Discrete Sample-Time
Constant Active Power	TP Resistive Load (0.5 kW)	H108	One Day ~ 1440 mins	100 ms / 100 µs
Voltage / Current Comparison (phasor and discrete) and power exchange at interface bus	TP balanced load profiles with a temporal resolution of 1min			
In Discrete Domain: PV feed-in at unity pf at interface bus	SP PV profiles with a temporal resolution of 1 min (6.7 kWp / phase)			

4.3.1 Scenario-1. Constant Active Power with a Resistive Load

In the first scenario, a constant TP resistive load of 0.5 kW is connected at the interface bus or PCC in discrete domain. The voltage and current should be in phase representing a pure active power being drawn by the load. The idea behind is to observe whether the waveforms are purely in phase or a there is any sort of delay due to the partition of the network and equivalent sub-system representations. The result from the simulation is shown in the **Figure 4.4** below:

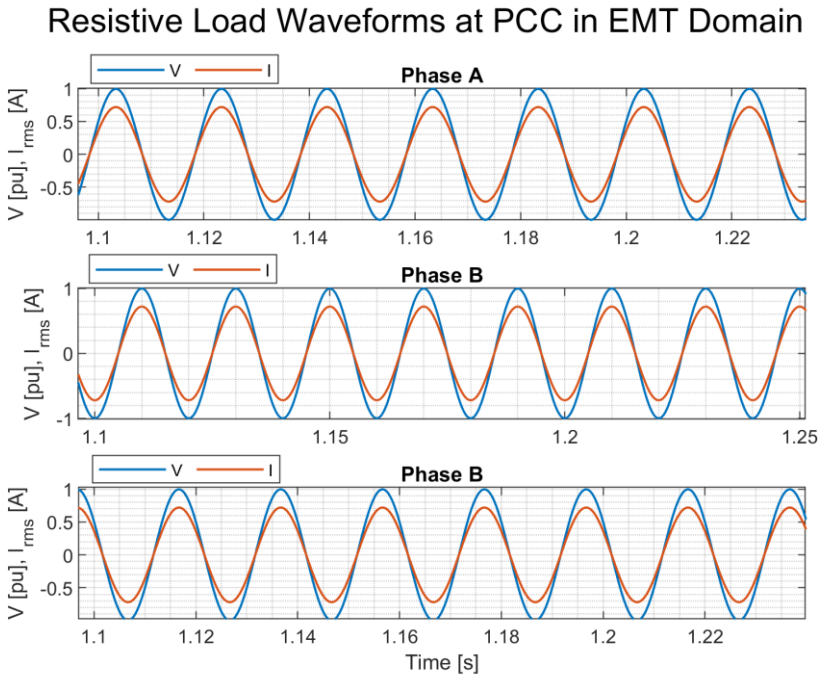


Figure 4.4 Voltage and current waveform for a pure resistive load.

The waveforms from the **Figure 4.4** above represents an ideal resistive load. The voltage and currents are completely synchronized and in phase with each other as observed at the zero crossings. This presents an insight into the functioning of the hybrid model in case of a conventional load. The results show that there seems to be no lag or delay and the exchange of variables at the interface is carried out smoothly.

4.3.2 Scenario-2. Voltage / Current Comparison and Power Exchange at the Interface Bus

To further observe the fidelity of the hybrid model, the voltage at the interface bus is compared from both the domains. In principle, the phasor voltage at the interface bus transmitted to the discrete domain should generate the waveform of the same amplitude. Similarly, the fluctuations should also be captured in discrete domain at the same time instant.

For this scenario, A TP load block from Simulink is connected at the interface bus in EMT domain with an external per minute profile. It represents a conventional TP uni-directional load. The voltage and current comparison is shown in the **Figure 4.5** below:

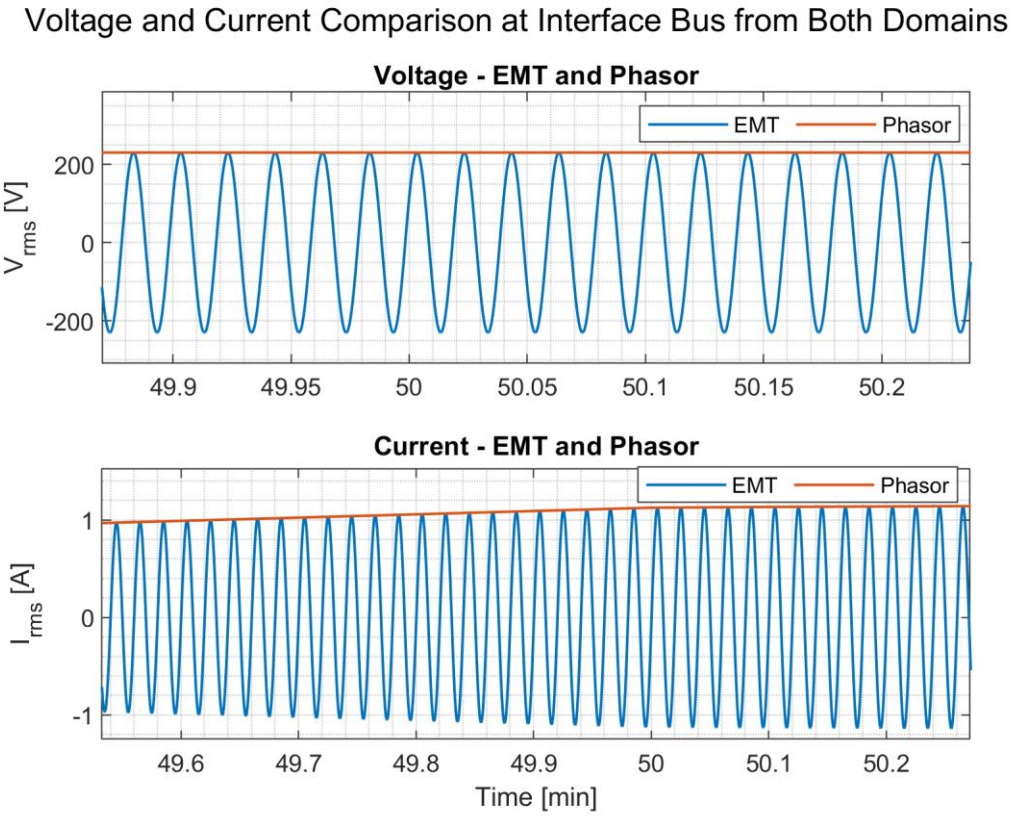


Figure 4.5 Voltage and current (rms) comparison at the interface bus.

The first sub-plot shows the comparison of the rms voltage measured from both domains at the interface bus. The second sub-plot shows the rms current, respectively. Both the phasor current and voltage follows the waveform, with the peak coinciding with the phasor values. In the second subplot, it can also be observed that there is a slight variation in current phasor values which is also followed by current waveform. The change in phasor magnitude is captured dynamically at the same instant as seen by the waveform results.

As a dynamic load is connected, so the powers exchanged / transferred between the two sub-models should also be the same. To observe the flow of power, the power drawn at the interface bus 108 in phasor domain is analyzed. The power values should be the same as demanded by the load in discrete domain. The power profile is illustrated in the **Figure 4.6** below:

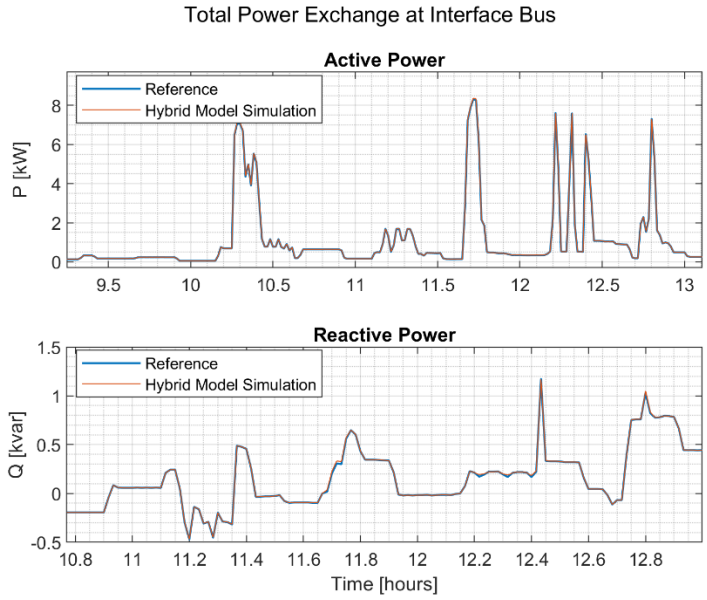


Figure 4.6 Power exchange at the interface bus.

The power profile for one complete day is observed. The above figure shows a zoomed in plot to visualize the power response of hybrid model compared to the reference. The reference power is simply the integrated load profile for the TP load. The power being drawn by the load connected in discrete domain exactly follows the reference. This exhibits that there is no illusionary power being transferred from phasor domain. It illustrates an ideal scenario. The voltage and current are the same at the interface bus in both the domains with no difference in magnitude and consequently the power consumed is also in accordance with the load profile.

4.3.3 Scenario-3. Feed-In at the Interface Bus with Unity pf Control

From the first scenario it can be apparently established that both the sub-systems are operating in synchronization. From the second scenario, the performance of the hybrid model is observed with a dynamic load connected at the interface bus. In this scenario, an additional feed-in per power profile is integrated at the interface bus in discrete domain to model a bi-directional power flow.

As the current will be injected into the system during feed-in, the idea is to first observe the fluctuations due to feed-in in phasor domain and the effect of same in generated waveforms in discrete domain. Secondly, the power values at the interface bus are observed in phasor domain depicting the reverse power flow due to the feed-in from discrete sub-system. The comparison is shown in the **Figure 4.7** below:

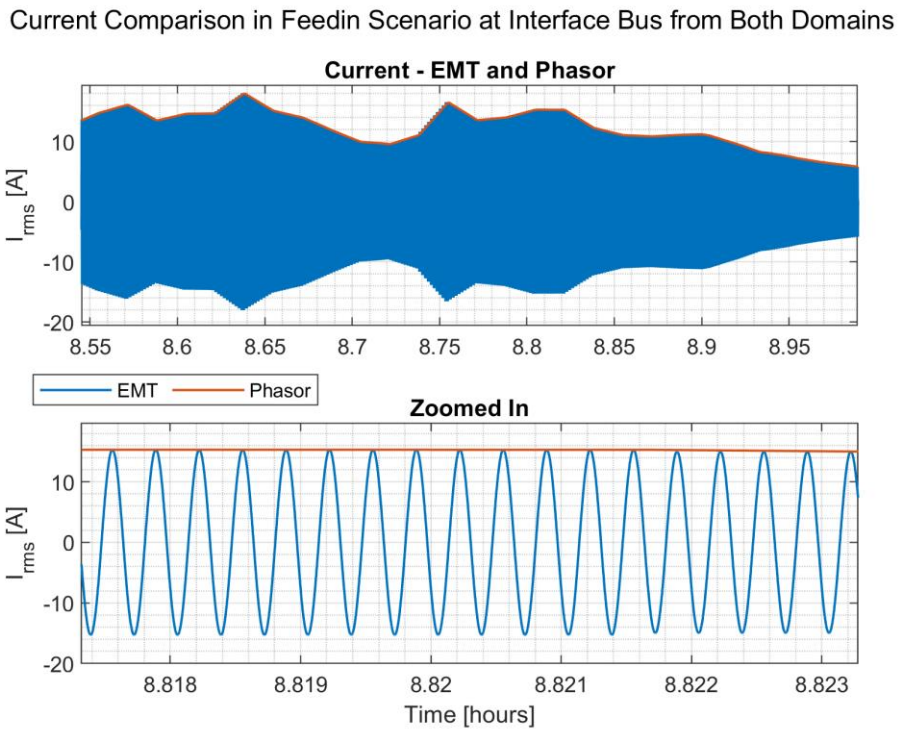


Figure 4.7 Current comparison at the interface bus during feed-in.

The first sub-plot in **Figure 4.7** above shows the fluctuations in the current magnitudes during the feed-in hours. It is observed that the waveform also exhibits instant fluctuations based on the rms phasor values. The follow-up is quite smooth as the rms values coincide with the peak of the waveform. The second sub-plot is a zoomed-in version to support the statement. The power profile is shown in **Figure 4.8** below:

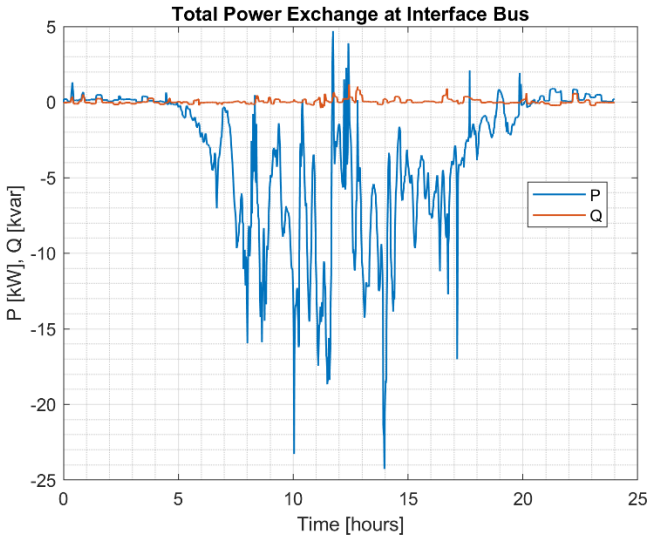


Figure 4.8 Total power at the interface bus.

The power profile illustrated in the graph above is measured at the interface bus in phasor domain. The blue plot represents the active power and it can be observed that during mid-day the reverse power flow is present. It shows power injection into the phasor network due to a feed-in source connected in discrete sub-system which would also affect the voltage magnitude at the interface bus,

respectively. Similarly, the reactive power consumption is due to the connected load profile and no additional reactive power is being consumed / injected.

The relevance of the hybrid model can now be understood practically with respect to PHIL simulation. From the results we can see that the voltage waveform at the interface bus in discrete domain can be obtained and will be sent to the RT simulator as reference V_{pcc} signal for the power interface. Likewise, the measured current waveform of the HUT will be treated in discrete domain to extract current phasor values. It will be then transmitted as a control signal for equivalent current sources to close the PHIL loop.

4.4 Summary

The design of the hybrid simulation in the Simulink platform is presented at length. Three different scenarios are implemented to get more insight on the functioning of the hybrid simulation. The results from all the three scenarios evidently show that the hybrid model is running in synchronization , the equivalent model representations using Thevenin and Norton circuits does not introduce any significant fluctuations or delay in voltage and current at the interface bus and finally the exchange of powers in both uni-direction and bi-direction case is ideal without the presence of any illusionary powers.

5 Power Hardware-in-the-Loop Simulation Setup

The workflow of simulated virtual LV grid model on Simulink interlinked with RT target machine is shown in the **Figure 5.1** below.

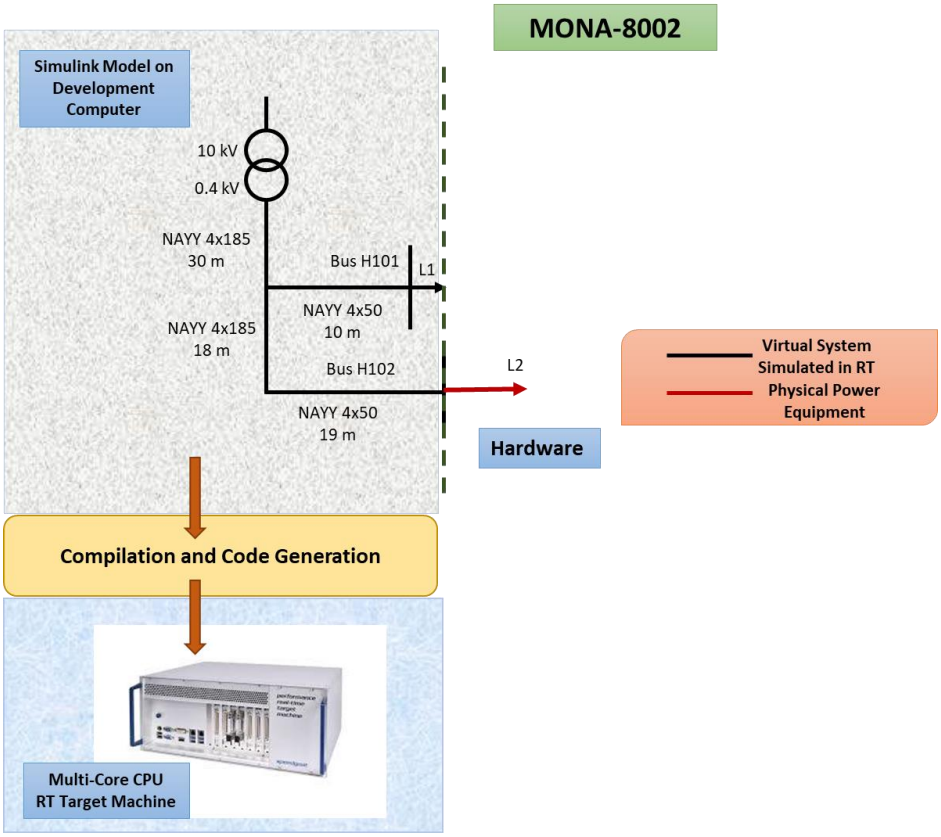


Figure 5.1 Structural workflow for model execution on RT target simulator.

The PHIL test procedure is scripted in detail in the following sections. The introduction to the components being used to perform the PHIL test are already mentioned in **section 2.3.1.2.** The interface method used in this study is also introduced briefly in **section 2.3.1.** It highlights which signals will be exchanged between the real-time system and the external power equipment. The Ideal Transformer Interface model interface is shown again in the **Figure 5.2** below in more detail with resemblance to the respective hardware components used for this study.

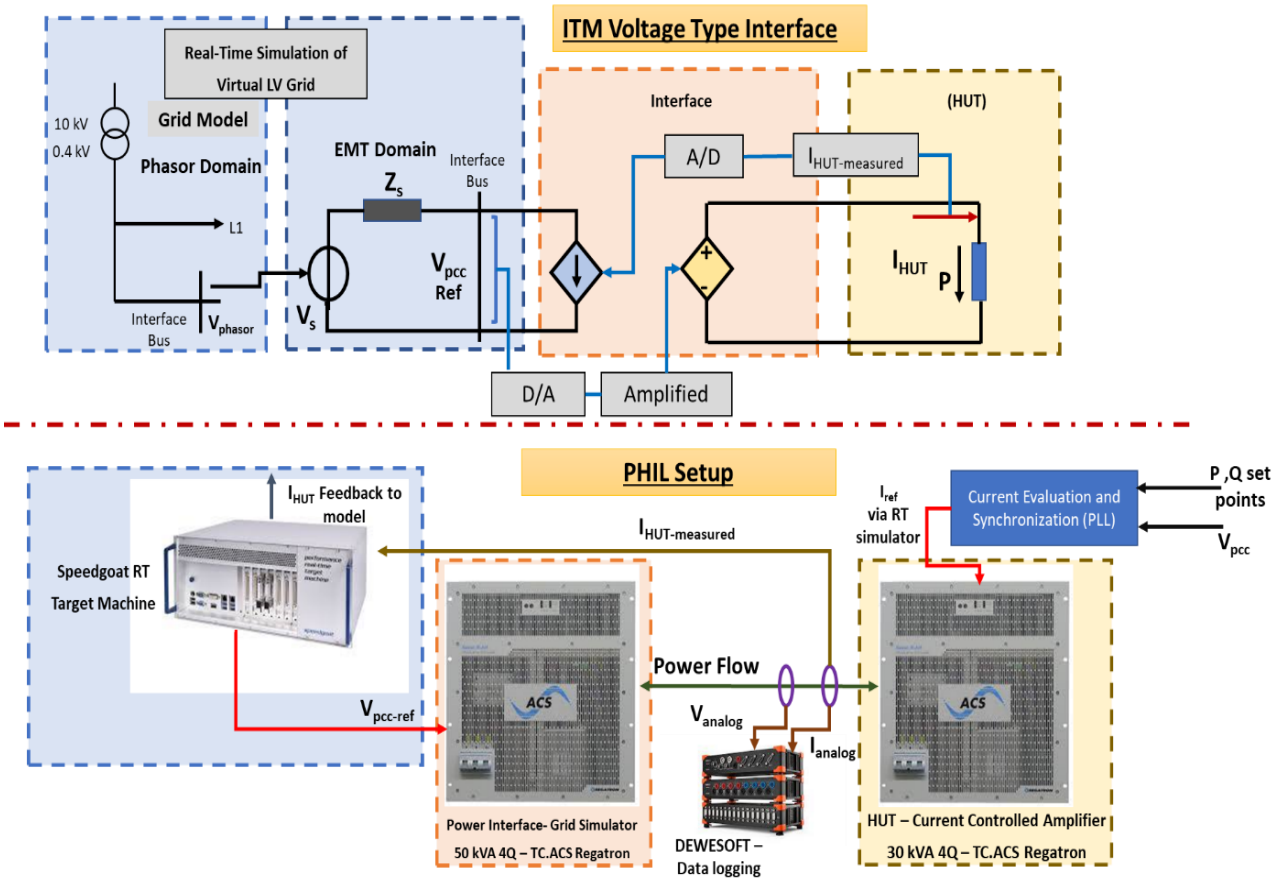


Figure 5.2 Complete PHIL test setup components in accordance with the ITM interface.

General functioning of the PHIL setup with respect to the **Figure 5.2** shown above is explained further. The top part above red dotted line of the figure represents the PHIL ITM voltage type interface while the bottom part represents the respective components being used in the test setup. For convenience, the components in the bottom part of the figure are enclosed with the same color dotted -line box as in the upper part indicating its functioning. The grid network part shown in the RT simulation box is modelled in RT on Speedgoat simulator. The $V_{pcc\text{-}ref}$ is the voltage signal at the interface bus from the virtual simulated grid. This digital signal is scaled down and converted to analog signal by the RT simulator. It is sent to the voltage-controlled power amplifier operating as power interface / grid simulator, depicted as a controlled-voltage source in ITM interface shown in **Figure 5.2** above. The grid simulator which is interfaced with the HUT amplifies the voltage to the nominal values. The operation of the HUT as load or feed-in is defined by the reference current signal I_{ref}, which is synchronized with the $V_{pcc\text{-}ref}$ and is evaluated based on power set-points. The I_{ref} is scaled down and sent via RT simulator to the HUT. The analog current (I_{analog}) that flows between the two amplifiers is measured externally, scaled down and sent to the real-time simulator to have the actual line current in the virtual model. This signal is then fed back as a control signal to the controlled-current sources in the model to close the PHIL loop. The actual power flow, V_{analog}, $V_{pcc\text{-}ref}$ and I_{analog} are logged using DEWESOFT data measurement device.

The scaling factors for D/A and vice versa are stated in the **Equations(17)** and **(18)** below. For the RT system outputs: a voltage of 10 V_{pk} refers to a 432 V_{pk} from the grid simulator output. Similarly, a current of 10 A_{pk} refers to a 20.4 A_{pk} from the grid simulator and vice versa. Based on this scaling factor,

the conversion formula used for voltage and current signals is defined below for the power interface and the HUT.

For 50 kVA Power Amplifier (Grid Simulator):

$$Actual\ Voltage_{pk} = \frac{432}{10} * V_{RT};\ Actual\ Current_{pk} = \frac{204}{10} * I_{RT} \quad (17)$$

For 30 kVA Power Amplifier (HUT):

$$Actual\ Current_{pk} = \frac{122}{10} * I_{RT} \quad (18)$$

For example, a reference of 1 V_{pk} from the RTS will generate an output of 43.2 V_{pk} from the grid simulator. The scaling relation of 1:1 is selected from the user interface for both the amplifiers indicating the same relation of input to output units, in this case for grid simulator it is volts (V) and for HUT it is amperes (A).

5.1 PHIL Laboratory Procedure

Before defining the scenarios, the start-up procedure of the complete setup is explained in this section. The PHIL simulation environment is shown in a layered diagram below with the measured signals of interest.

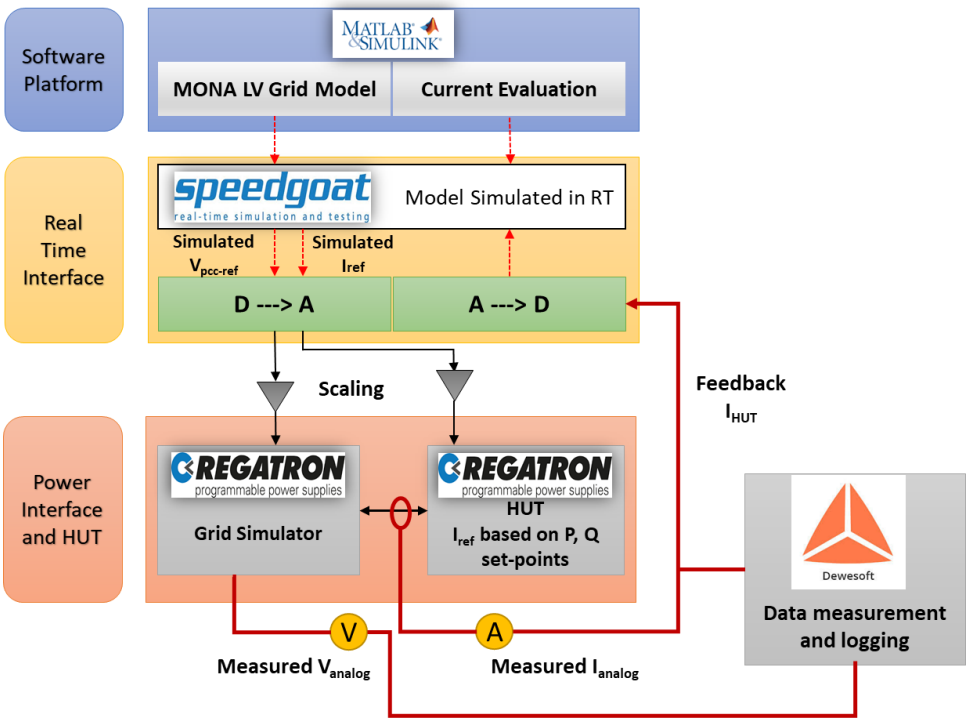


Figure 5.3 PHIL simulation environment.

5.1.1 PHIL Start-up and Execution

The step by step execution of the hardware setup is listed below:

- The simulated LV network modelled in Simulink platform is compiled in real-time by setting the simulation mode to external. After the model is built on the Speedgoat RT target machine,

the simulation is executed which produces a scaled down voltage reference signal for the power interface.

- The grid simulator produces the amplified voltage at its terminals based on the set-points received by the RT simulator. For the power interface, the voltage-controlled mode is selected from the Regatron's user interface. The voltage limits must be cross checked before switching-on the amplifier and also the rms values. This is enabled by the DEWESOFT device user interface on which the signal statistics can be analyzed. The following **Figure 5.4** displays the user interface of power amplifier with the mode set to voltage controlled to operate as grid simulator outlined in red box.

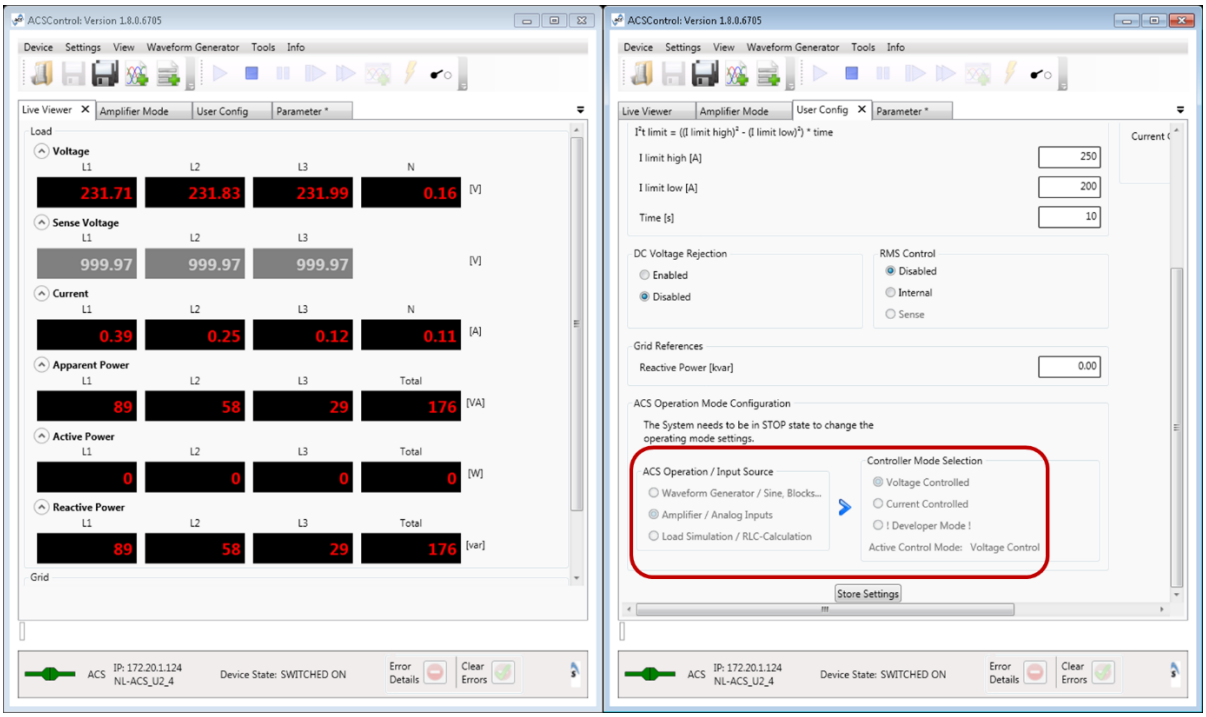


Figure 5.4 Snapshot of Regatron user interface for voltage controlled power amplifier.

- After the voltage is successfully established, the scaled down reference current command can be sent to the RT simulator. The HUT is operated in two modes namely the amplifier mode → current controlled and also RLC load simulation mode. This can also be done via Regatron's user interface. The application of both operational modes is explained in the following sections. The AC voltage at the grid simulator can now be applied to the HUT by switching it on. In this manner, the external power connection between the grid simulator and the HUT is established. In current-controlled mode the HUT is expected to draw the current as commanded from the RT simulator while in RLC load mode the current drawn by the HUT depends upon the respective RLC configuration set via the device interface. The following **Figure 5.5** displays the user interface of power amplifier with the mode set to current-controlled to operate as HUT outlined in red box.

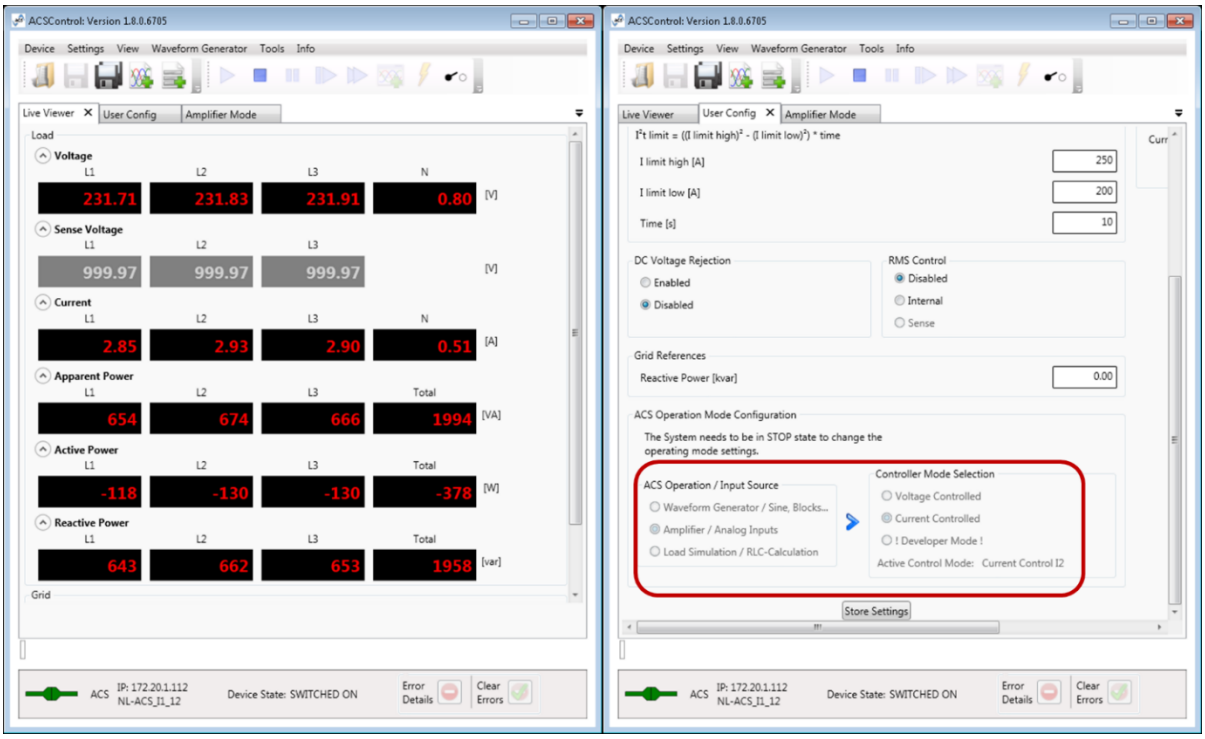


Figure 5.5 Snapshot of Regatron user interface for current controlled power amplifier.

- The measurements (current and voltage) are logged externally by means of data measurement devices from DEWESOFT. Additionally, the current measurements of the HUT are fed back to the RT simulator after scaling it down within the desired range using **Equation (17)**. The currents can be obtained directly from the out ports of the amplifier by establishing a connection from respective current out ports of the device to the RT simulator.

- The injection of acquired external currents to the controlled-current sources modelled in Simulink closes the PHIL loop. The feedback signal is first treated in discrete domain to extract the instantaneous phasors and then transmitted as a control signal for the sources modelled in phasor domain.

The sampling rate of the data measured in real-time by the DEWESOFT devices are defined in the **Table 8** below. Datasheet of the analog specifications of DEWESOFT device is shown in **Appendix B.3.**

Table 8. Data acquisition sampling rates.

Variables	Sample Rate (Hz)
Continuous Signals	
Voltage	100 k
Current	100 k
RMS values	
Voltage	10
Current	10
Power	5
Frequency	3.1

The description of the PHIL scenarios is outlined in **Table 9** below. The complete close loop PHIL is not implemented right away rather the scenarios are built on its predecessors in complexity. The scenarios are implemented on MONA-8002 network.

Table 9. PHIL Simulation Scenarios.

Scenarios	HUT	Connection at PCC	Interface Bus	Sample-Time
Open Circuit Voltage				
Real-Time Voltage Control	No	Open Circuit	H102	100 µs
Close Loop PHIL				
Real-Time Current Control	Configured in RLC Load Simulation Mode	Resistive Load	H102	100 µs
	Current-Controlled Amplifier Mode Configuration	I_{ref} from the model based on resistive power set-points		
PHIL With A Constant SP Load	SP Load Bank	Constant Resistive Load		
Methods for Improvement of HUT performance	Current-controlled Amplifier Mode Configuration	I_{ref} with a time delay through static and dynamic compensation		

5.2 Scenario-1. Real-Time Voltage Control

The first scenario is tested to observe the response of the power interface i.e. the grid simulator. It will help to establish the characterization of the power interface to find out the associated errors, noise, or delay. In this scenario the aim is to observe whether the commanded reference voltage signal sent by the RT simulator is followed by the power interface or not. Bus H102 is chosen as the interface bus. In discrete domain sub-system, the Thevenin equivalent system is represented by a controlled voltage source and an equivalent impedance. No load is connected at the interface bus as the aim is to just test the follow-up of reference voltage signals by the power interface. Basically, the scenario can be referred to as an open-circuit voltage test. The following **Figure 5.6** illustrates the arrangement of the hardware test setup for this scenario.

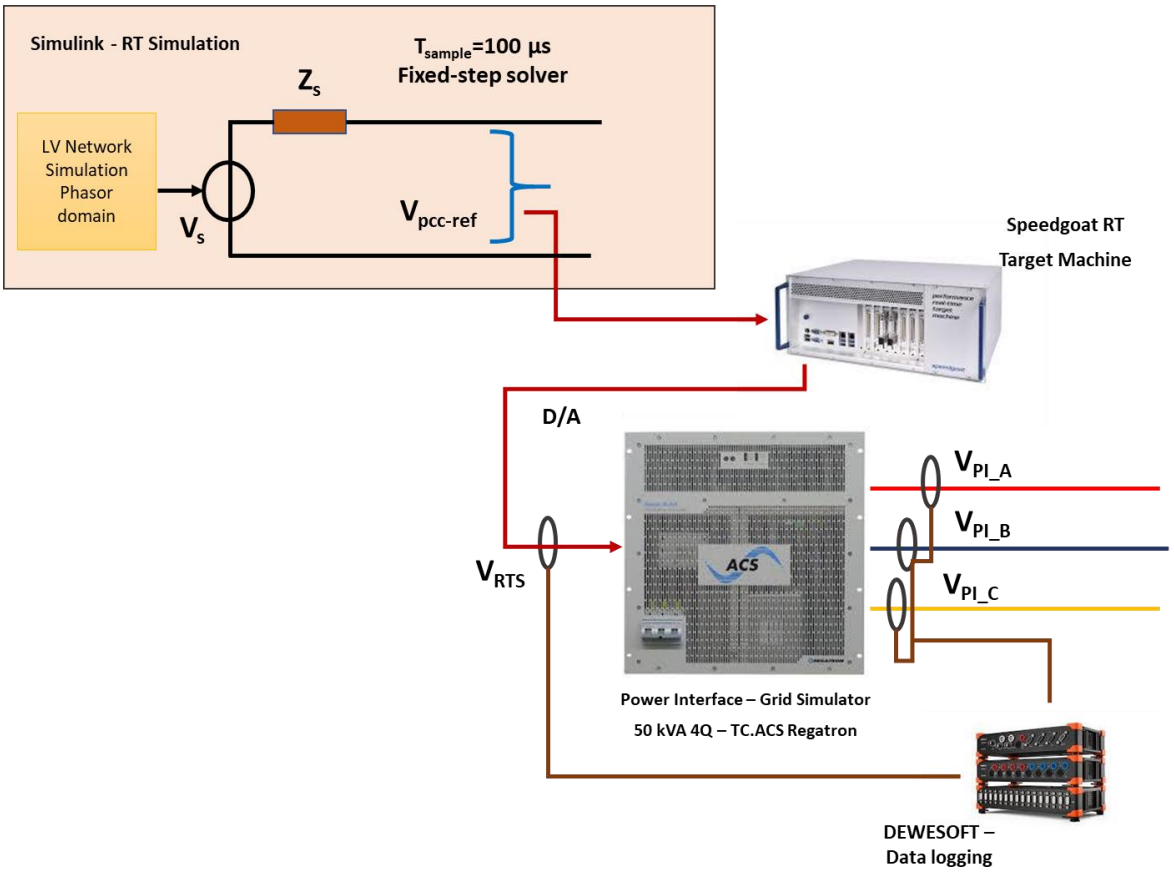


Figure 5.6 Test setup for the first scenario.

The scaled down voltage values ($V_{pcc-ref}$) at the interface bus from the simulated network are passed on as a reference signal (V_{RTS}) from the RT simulator to the interface. Comparison is performed between the reference analog voltage output of the RT simulator and the measured amplified voltage output of the power interface. Both waveform and the RMS values are compared to acquire a better overview. V_{RTS} is multiplied by the scaling factor 43.2 V, for the convenience of comparison with the measured interface output.

Parameters set in this scenario are:

$V_{RTS\text{-}nom}$ = 400/sqrt (3) V_{rms}; Sample Time = 100 µs; Z_s= [0.0218 Ω, 68 µH]; No load at Bus # H102.

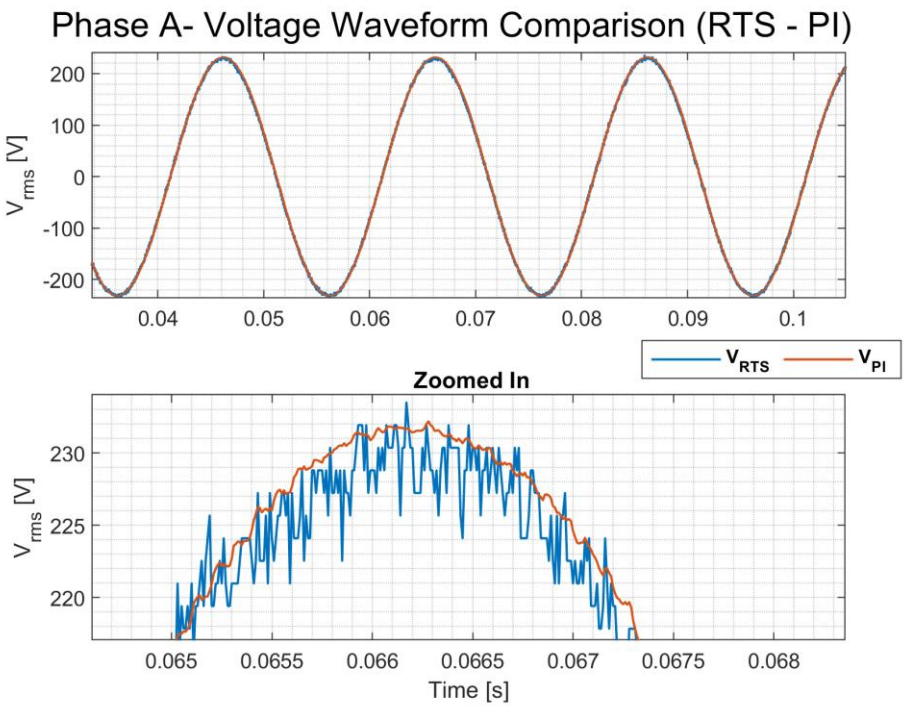


Figure 5.7 Voltage waveforms showing follow-up of V_{ref} by the power amplifier.

From the zoomed out first sub-plot of the voltage in **Figure 5.7**, it seems like the reference voltage signal (V_{RTS}) is accurately superimposed by the interface output (V_{PI}). The output is completely in phase with the reference voltage from the RT simulator. The second sub-plot is a zoomed in version of the first sub-plot at the peak voltage. From this, the noise associated with the RT simulator output can be easily distinguished. The interface's output voltage is much smoother than the simulator output. The RT simulator sends an output at each time-step and the model is simulated at a discrete time-step of 100 µs. The simulator output would probably get better with a higher discrete sample time. The sample time of 50 µs was tried but due to computational limitation of the RT simulator the "CPU overload" error was produced, and the simulation was not executed. The sample-times of as low as 5-10 µs are desired for better accuracy of reference signals. As far as the power interface is concerned, the default built-in filters eradicated the noise to some extent and the output appears out to be smoother. The voltage phase angles from the simulated model and from the power interface are also observed as shown in the **Table 10** below to analyze if there is a delay.

Table 10 Voltage phase angles.

	V_{RTS}	V_{PI}
Phase A	0	0
Phase B	-120°	-119.99°
Phase C	120°	120.03°

There is a minute difference in the phase angles observed in phases B and C. This indicates that a time delay is involved between the V_{RTS} and $V_{PI.}$ To have better insight about the voltage magnitudes, the rms values are plotted as shown in the **Figure 5.8** below.

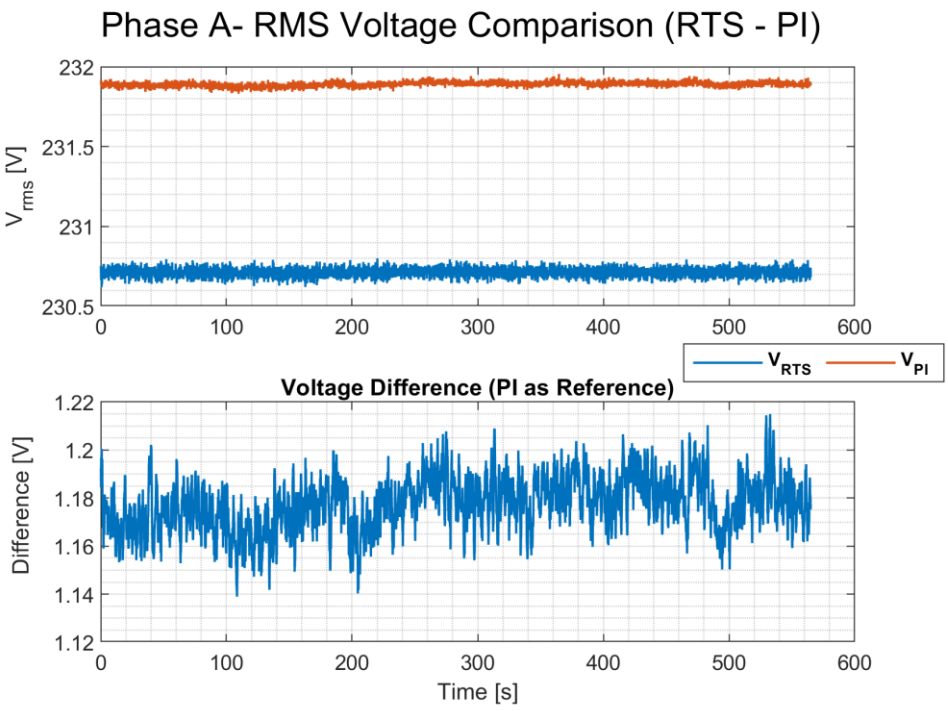


Figure 5.8 Reference V_{rms} value by the RT Simulator and the interface output.

As evident from the graph in **Figure 5.8** above, there seems to be a difference in the rms voltage magnitude commanded by the RT simulator to the magnitude measured at the output of the power interface. A constant offset of around 1.17 V_{rms} is observed.

5.2.1 Step Response to Examine Voltage Offset

To examine whether the offset is constant, an interim voltage offset analysis test is performed. A balanced three-phase voltage source is connected with a series impedance to model a simple circuit. The voltage at the output nodes of the circuit is observed. The step function is used at the source input to step-up the nominal voltage amplitude after a certain time period. This is done to observe whether the offset remains constant throughout in an event of dynamic change in voltage. The following **Figure 5.9** shows the simple circuit developed in Simulink to conduct the voltage offset test. It is a simple Thevenin equivalent representing the MONA-8002 grid with the same impedance parameters. The voltage-controlled source signal comes from a sine wave generator block which enables to vary the amplitude during the simulation. The V_{RTS} is the reference open circuit voltage passed on to the power interface through RT simulator.

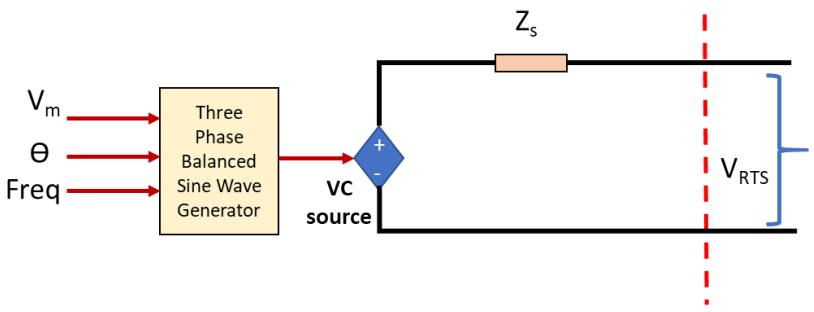


Figure 5.9 Model developed to test voltage offset of the power interface.

Parameters set in this scenario are:

Model Simulation Time =200; At T=0 → $V_{RTS\text{-}nom}$= 215 V_{rms}; At T=100 → $V_{RTS\text{-}nom}$= 230 V_{rms}; Z_s=[0.0218 Ω, 68 µH] ; Sample Time= 100 µs; No load Connected at Bus # H102.

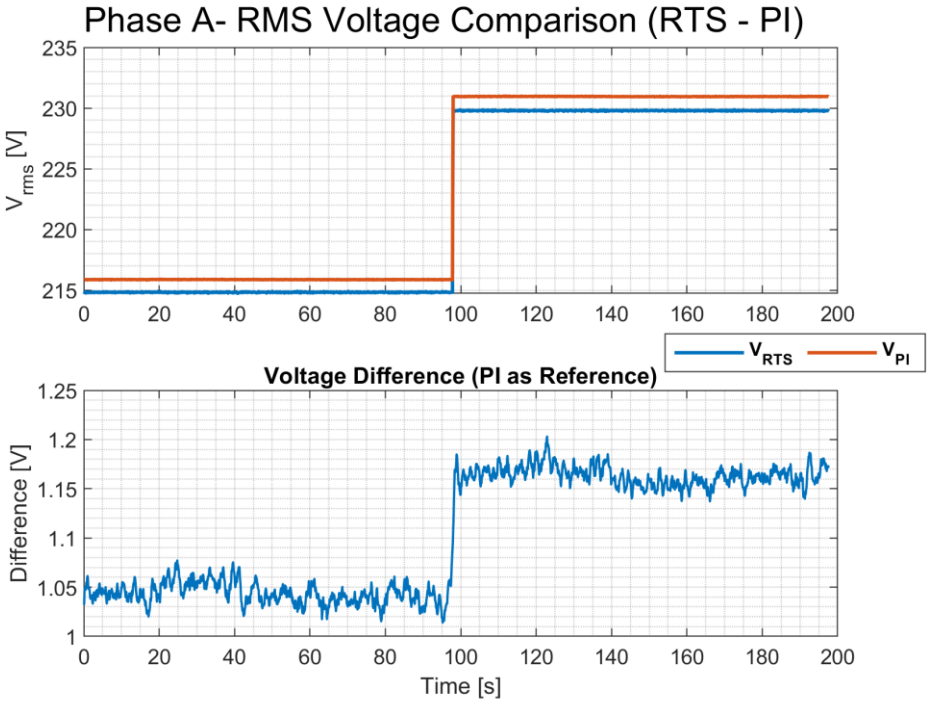


Figure 5.10 Voltage offset analysis with a step response.

From the first sub-plot, it can be seen that the V_{RTS} is changed from 215 V to 230 V halfway through the simulation. The measured output voltage of the interface also follows up this step response. However, the second sub-plot shows the difference between V_{RTS} and V_{PI}. The offset does not remain constant and has changed slightly with the reference voltage magnitude. At an input of V_{RTS}=215 V_{rms} it is 1.05 V whereas when the input is stepped up to V_{RTS}=230 V_{rms} the offset has increased by 0.1 V. This opens up the possibility of a direct relationship between the power interface offset and the V_{RTS} magnitude.

5.2.2 In-Depth Analysis of Power Amplifier's Voltage Offset

The same model as shown in the **Figure 5.9** is used to obtain more insight regarding the voltage offset. The reference voltage from the RT simulator is now dynamically varied after a certain time interval in steps of 25 V_{rms} during the execution of the model in real-time. It starts from 50 V_{rms} and stepped-up until it reaches 300 V_{rms}. Throughout, the interface output is measured and the difference between the commanded V_{RTS} and V_{PI} is evaluated. The following graph in **Figure 5.11** shows the result.

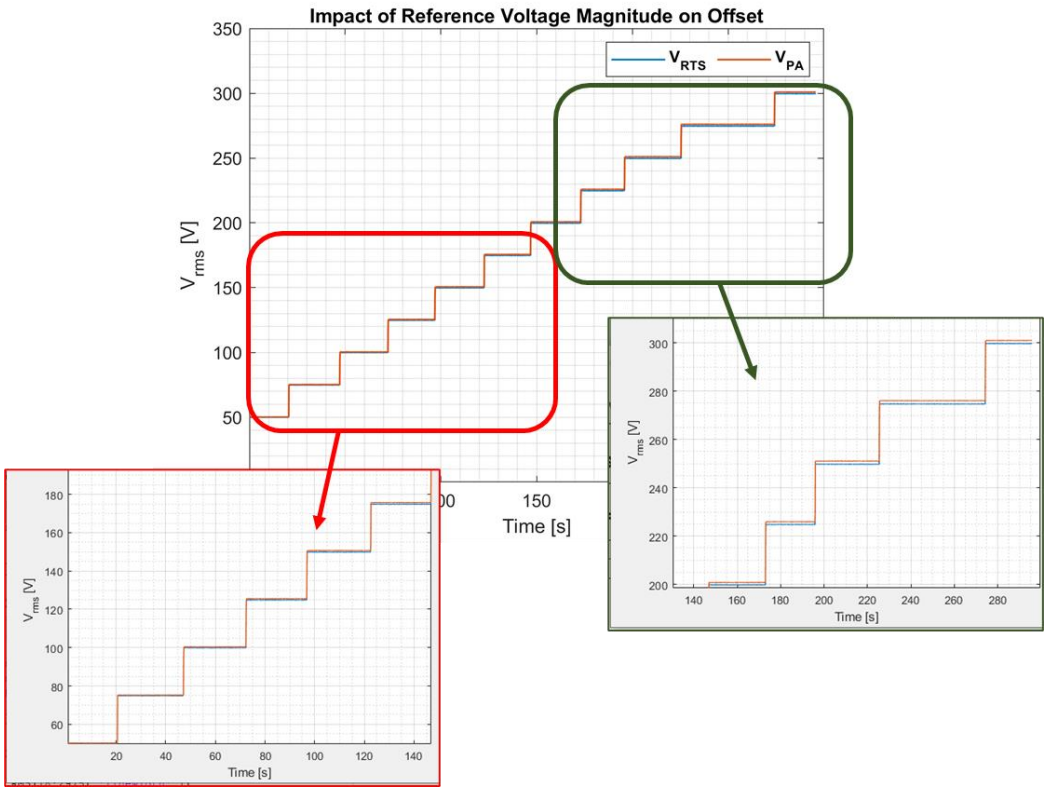


Figure 5.11 Power Interface output with increasing V_{ref} from the RTS.

The step graph above shows the voltage commanded from the simulator and the corresponding measured power interface output. In the red highlighted box, the first half of the main graph is zoomed-in, it is apparent that the V_{RTS} and V_{PI} almost overlap initially exhibiting little or no difference at all. As the voltage is increasing, the two gets more distinguishable as shown in the green highlighted box, zooming in the second half of the main graph. The offset is therefore increasing. The following graph explicitly illustrates the pattern.

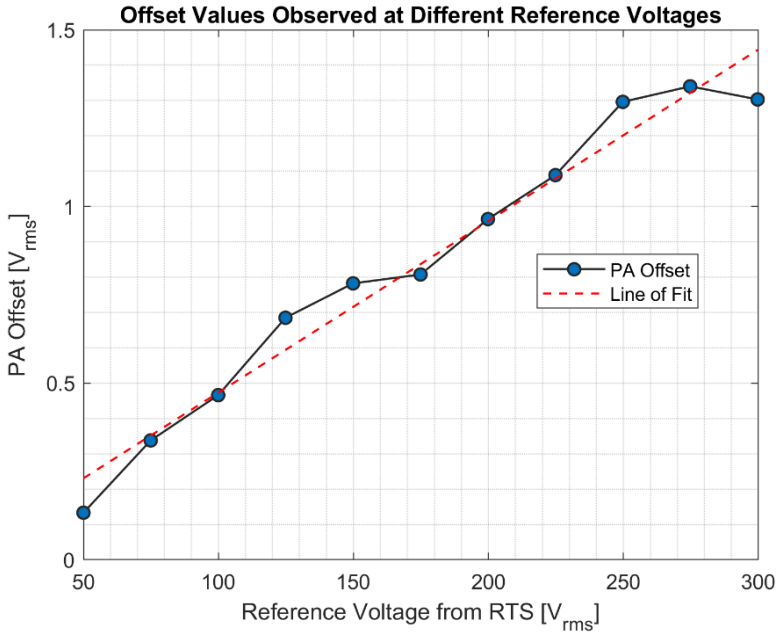


Figure 5.12 Relation between V_{ref} from RTS and PI offset.

An almost direct impact on voltage offset is thereby observed with the increasing V_{RTS} as shown from **Figure 5.12** above and the obtained line of best fit is shown as a red dotted line. At V_{RTS}=50 V_{rms} the offset is fairly low around 0.2 V and the power interface outputs the same voltage as commanded by RT Simulator. The offset increases to a significant 1.15 V_{rms} at the standard V_{rms} = 230 V and continues to increase further. Interestingly a dip is observed in the offset at the end when the V_{RTS} is the highest i.e. at 300 V. At 275 V_{rms}, the offset is approximately 1.35 V whereas at 300 V_{rms}, it is lowered to 1.3 V. Probably at a certain high input, the difference between the V_{RTS} and V_{PI} becomes constant and does not increase further. This could be theoretically correct but to get a firmer understanding the values at higher reference input voltages are desirable. In this case, it is not attempted due to the voltage limit violation of 305 V_{rms} for the PI. Nevertheless, the findings assert that between the operational value of 0 – 275 V_{RTS} there exists an increasing offset between V_{RTS} and V_{PI}. As V_{RTS} increases the offset from PI becomes significant. The following **Equation (19)** of the line of best fit can be used to approximate the rms offset from the PI at a certain reference input from the RTS.

$$\text{Offset}_{\text{PA}} = 0.0049 * V_{\text{RTS}} - 0.012 \quad (19)$$

From the **Equation (19)** above, it is obvious that for a low reference input, the PI will output approximately the same voltage. The following **Table 11** shows the comparison of actual offset measured and the values obtained through the line of fit equation.

Table 11. Offset values from Line of Fit equation.

Voltage from RTS (V_{rms})	Actual Offset from PI (V_{rms})	Value from Fit Equation (V_{rms})	Fit Error (V_{rms})
50.01	0.13	0.23	0.10
74.90	0.34	0.35	0.01
99.90	0.47	0.47	0.01
124.83	0.68	0.59	-0.09
149.87	0.78	0.72	-0.07
174.86	0.81	0.84	0.03
199.82	0.96	0.96	-0.01
224.83	1.09	1.08	-0.01
249.78	1.30	1.20	-0.10
274.74	1.34	1.32	-0.02
299.72	1.30	1.44	0.14

The error produced by the line of fit equation is very minimal except for the last value at the reference input of approx. 300 V_{rms} as already discussed. However, the equation is promising to obtain the offset of PI (grid simulator) between the reference inputs range of 75 – 275 V_{rms}.

5.3 Scenario-2. Real-Time Current Control

After analyzing the performance of the grid simulator, the response of another power amplifier (i.e. HUT) operating in current-controlled mode needs to be tested. The response of the HUT based on the reference current signals is very significant. The reference current injection signals for the HUT are evaluated based on power set-points and voltage at the PCC. The following **Figure 5.13** illustrates the simplified process flow behind the evaluation of reference three-phase injection currents for the HUT. The three -phase voltage splits into direct and quadrature axis values inside the discrete three-phase PLL block. It is further treated to calculate the frequency and wt of the signal respectively by means of

a variable frequency block and PI controller. The discrete three-phase PLL block is part of the three-phase dynamic load block mask in Simulink and is developed by P, Girroux and G, Sybille from the Power System Laboratory, IREQ, Hydro-Quebec. Detailed model of the respective Simulink block is shown in **Appendix C**.

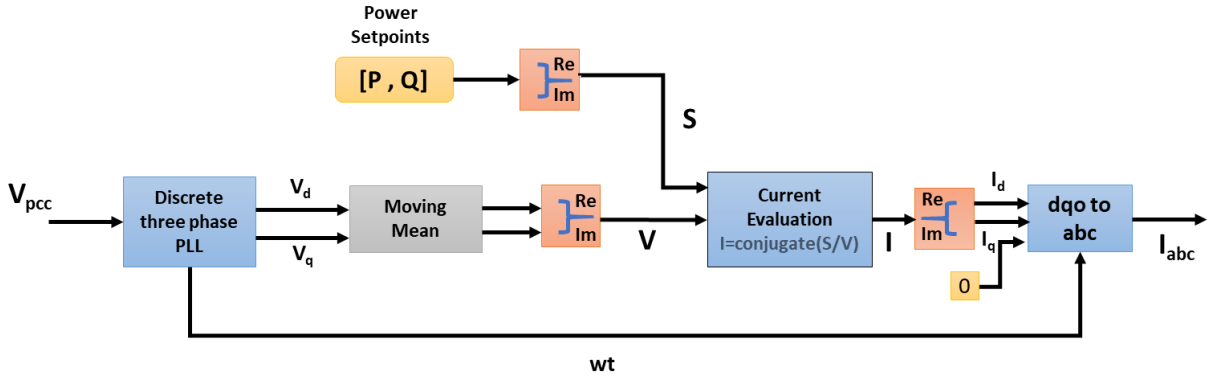


Figure 5.13 Reference I_{HUT} evaluation based on power setpoints and V_{pcc} using Discrete three-phase PLL block.

In this scenario, the capability of the HUT is analyzed to follow up the commanded reference current signals and to observe the pure active power flow for a resistive load. If the current waveform generated by the HUT does not follow the reference signals properly there could be unwanted illusionary active and reactive powers. For this scenario, two approaches are followed. In the first one, the HUT is operated in an RLC load simulation mode with the configuration set to a constant resistive load. As stated earlier, the configuration can be opted via the Regatron's user interface. For the voltage waveforms, the same approach is followed as defined in the previous **section 5.2** i.e. V_{ref} values at the interface bus H102 of the MONA-8002 network is sent to the RT simulator. The HUT is connected with the grid simulator to establish the same phase voltages across its terminals. The idea is to observe and measure the current signals being drawn by the HUT. Being operated in a resistive mode it is expected to have a complete in-phase current waveform with the voltage depicting unity pf. The following **Figure 5.14** illustrates the arrangement of test setup for this scenario.

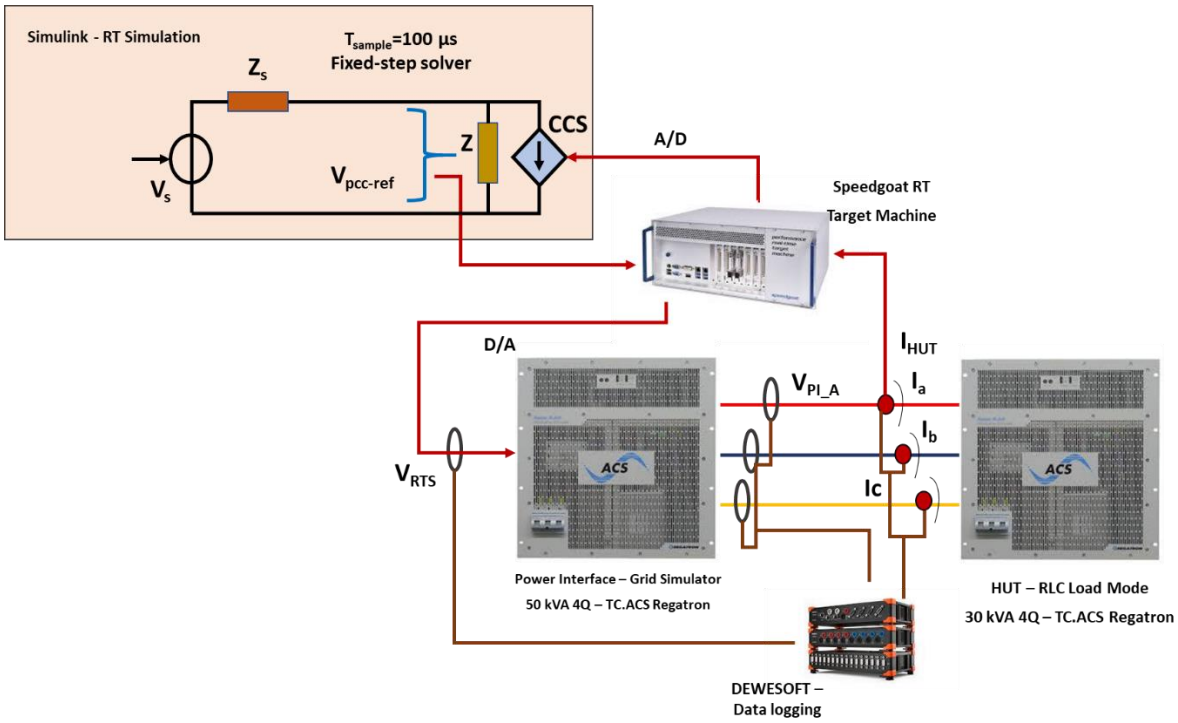


Figure 5.14 Test setup for the PHIL scenario with HUT in RLC load simulation mode.

Parameters set in this scenario are:

$V_{RTS\text{-}nom}$ = 400/sqrt (3) V_{rms}; Sample Time = 100 µs; Z_s= [0.0218 Ω, 68 µH]; HUT is operating in RLC load simulation mode with R_{HUT} = 30 Ω i.e. 10 Ω / phase.

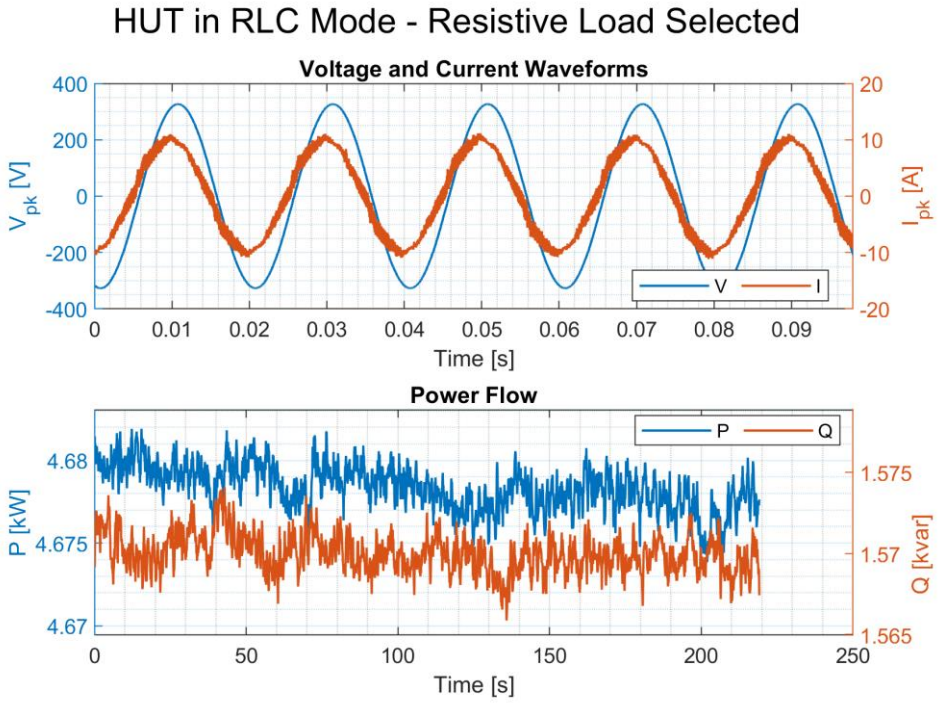


Figure 5.15 HUT response in RLC mode for a resistive load.

Ideally, for a resistive load the voltage and current should be in phase. But from the first sub-plot in **Figure 5.15**, it can be seen that it is not the case in fact the current is leading the voltage. The HUT is

operating as a capacitive resistive load with a leading pf of 0.95 whereas it should be unity. There is a phase difference between the voltage and current, based on the pf value the current is leading the voltage by 18^{o}. This contribute towards undesirable reactive power flowing into the grid. As shown in the second power flow sub-plot, there is a significant reactive power of approximately 1.57 kvar along with the active power. The HUT is supposed to draw only active power but, in this case, there is also a reactive power in the system which would affect the results when a controlled power injection is desired from the HUT. Concerning the active power, the resistive load is set to 30 Ω which should render to an active power of 5.33 kW with a nominal 230 V_{rms} / phase when the same load configuration is simulated offline. However, as seen in the power flow sub-plot, the power drawn is around 4.68 kW i.e. a deficit of around 0.6 kW. So, on top of undesirable capacitive reactive power the HUT is also not drawing optimum active power. To examine the characteristics of HUT further, another scenario is performed as defined below.

In the second approach, instead of operating the HUT in RLC load simulation mode it is being operated in the amplifier → current-controlled mode. The PHIL loop is closed by feeding the measured I_{HUT} back to the virtually simulated network through RT simulator after A/D conversion. The idea behind is to send the scaled down I_{ref} signals through RT simulator to the HUT (CC amplifier), calculated based on the power set-points to observe whether it follows up and acts as a resistive load drawing the same power from the grid. Two reference signals will now be generated from the virtually simulated network. First being the voltage (V_{RTS}) at the interface bus and second being the current (I_{ref}) for a resistive load of power (5.34 kW). The power value corresponds to a resistor of 10 Ω/phase as chosen for the previous scenario where HUT is operated in RLC load mode. Irrespective of the HUT operating in RLC load mode or current-controlled mode it should exhibit the same response as in both the cases the load configuration is the same. The test setup is the same as shown in **Figure 5.14,** the only change is the operating mode of the HUT from RLC load simulation to current-controlled amplifier. The reference current is evaluated in the same manner as shown in **Figure 5.13.**

Parameters set in this scenario are:

V_{nom} = 400/sqrt (3) V_{rms}; Sample Time = 100 µs; Z_s= [0.0218 Ω, 68 µH]; P_{ref}= 5.34 kW, Q_{ref}=0 kvar; HUT operating as current-controlled amplifier.

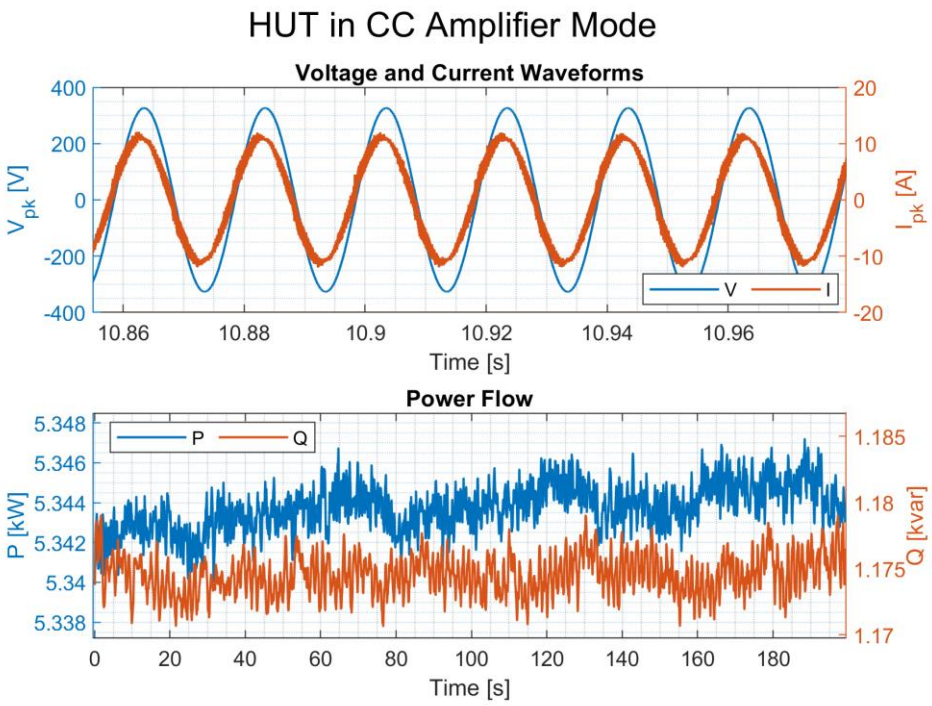


Figure 5.16 HUT response in CC amplifier mode for a resistive load.

From the first sub-plot in **Figure 5.16**, the waveform can be observed. The phase difference has improved as compared to the previous scenario but not completely. The current leads the voltage and a leading pf of almost 0.97 is measured, means that the HUT is still operating as a capacitive resistive load. Compared to the previous case, the reactive power has reduced by 0.4 kvar while the active power being drawn by the HUT is close to what is desired i.e. 5.4 kW. The performance of the HUT is improved while operating in CC amplifier mode and controlled externally via I_{ref}. However, still a significant undesirable capacitive reactive power is present in the system. This could be due to the parasitic capacitors being used in switched-mode power amplifiers behaving as low pass filters for the output. To understand the operation of the power components during the PHIL simulation, the power quadrants are observed as shown in the **Figure 5.17** below.

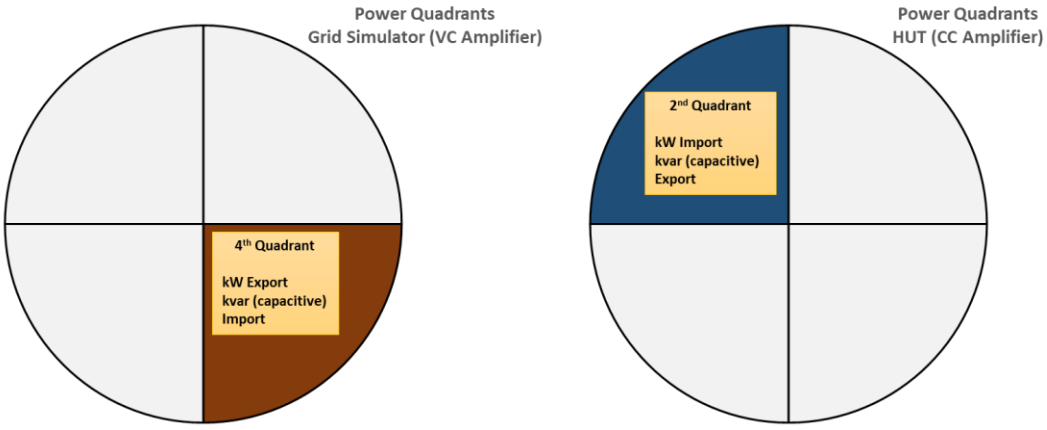


Figure 5.17 Power quadrants illustrating operation of grid simulator and HUT.

The grid simulator i.e. the power interface is operating in the 4th quadrant and the HUT is operating in the 2nd quadrant as highlighted in the **Figure 5.17** above. As per IEC 62053-23 explanation of the power quadrants, the 4th quadrant indicates the export of active power and the import of reactive power with a leading pf. So, the grid simulator is the source of active power for the HUT but at the same time it is receiving capacitive reactive power from the HUT. Similarly, the 2nd quadrant indicates the export of reactive power and import of active power. This is the case for the HUT, which explains that the HUT behaves as a source of capacitive reactive power and a sink for active power. The same behavior is observed in the results from 2nd scenario.

The HUT seems to have a default capacitance introducing reactive power in the system, in both the operation modes. To build-up on this and to approximate the value of the default capacitance, another test is performed. In this approach, the HUT is connected to the grid simulator operating in CC amplifier mode however this time no I_{ref} signals are being sent to the HUT. The idea is to observe the behavior of CC amplifier as a capacitive load when operated in idle condition and not being controlled externally to draw any power. The results are shown in the **Figure 5.18** below.

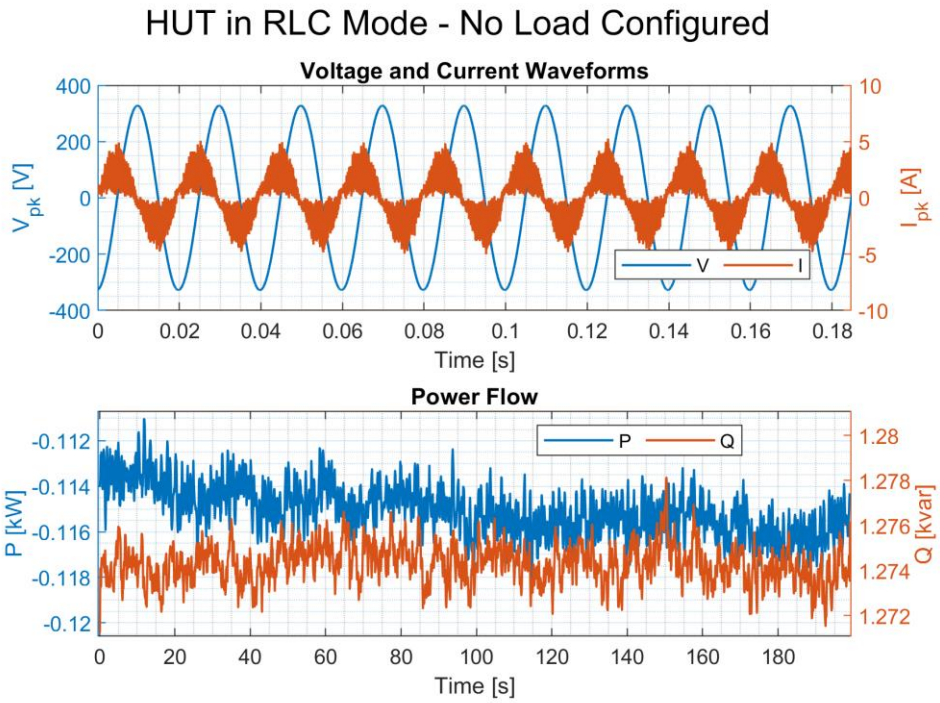


Figure 5.18 HUT response in CC amplifier mode with no external I_{ref} signal.

As expected, there is an I_{pk} of approximately 4A as seen from the distorted current waveform leading the voltage in the first sub-plot. The voltage is established along the HUT terminals as it is connected to the grid simulator, and the current flows in the system due to the capacitance of the HUT. From the second sub-plot, it is apparent that the HUT is not drawing any active power as desired but there is a capacitive reactive power of around 1.274 kvar being supplied from the HUT to the source i.e. the grid simulator. It is evident that the HUT is behaving as a capacitive load. Considering the power and voltage values from this scenario, the capacitance / phase is calculated as shown in the following **Equation(20).**

$$Q_p = \frac{{V_{rms}}^2}{Z_c} = \frac{232^2}{\frac{1}{2 * pi * 50 * C_p}} \rightarrow C_p = 25\ \mu F \quad (20)$$

The reactive power from the HUT is not constant rather varying with its operation in different modes as illustrated in **Figure 5.15** and **Figure 5.16.** Nevertheless, the value gives an approximation of the default capacitance of the current-controlled amplifier at standard voltage.

5.3.1 Impact of Voltage Level on Current-Controlled Amplifier (HUT) Capacitance

The value of parasitic capacitance obtained in **equation (20)** may hold true for standard voltage. To get more insight on the change of parasitic capacitance with increasing voltage, the same criteria as the last one with no external current control is performed means no active power is commanded by the HUT. This time the reference voltage at the interface bus being sent to the RT simulator is increased from 40 to 300 V_{rms} in intermediate steps. The following graph shows the result.

Parameters set in this scenario are:

V_{nom} → [40 to 300] V_{rms}; Sample Time = 100 µs; P_{ref}= 0 kW, Q_{ref}=0 kvar; HUT operating as current-controlled amplifier.

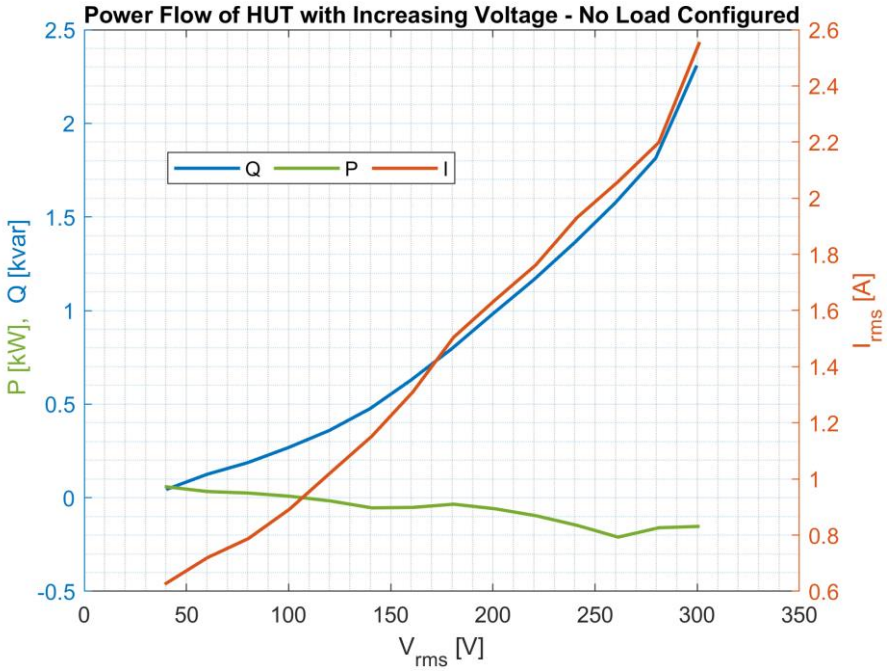


Figure 5.19 Impact of HUT capacitance with increasing voltage.

The green line in the **Figure 5.19** above shows the active power consumption of the HUT and as the commanded power setpoints are [0 kW, 0 kvar] the active power is almost negligible. Interestingly, the blue line represents the reactive power and with the increase in voltage the reactive power injection from the HUT side increases. At low voltage, there is no reactive power, however it increases significantly with voltage as explained by the current magnitude represented in red line. This explains that the effect of parasitic capacitance is also dependent on the voltage across HUT terminals. It behaves as a variable capacitive load to the source. At 300 V_{rms}, the reactive power is around 2.3 kvar. Thus, the effect of capacitance is very prominent and is not constant. If that would have been the case, it would be comparatively convenient to develop control algorithm. But from the aforementioned

results, it is evident that the capacitance effect will vary with the setup, operating mode of the HUT and commanded power setpoints.

From the analysis of real-time current control scenario in this section, the response and characteristics of the HUT has been analyzed in two different modes. It is established that the HUT behaves as a variable capacitive load and injects reactive power regardless of the fact that it is controlled externally or not. This reactive power should be compensated in order to achieve controlled power injection from the HUT. Furthermore, it will also impact the voltage levels undesirably and the response of Q-management cannot be analyzed accurately in real-time due to the presence of uncontrolled reactive power.

5.4 Scenario-3 PHIL with A Constant SP Load (Resistor)

In this scenario the HUT is replaced completely by a constant SP resistive load bank. In previous scenario, the problems associated with the HUT as CC amplifier are highlighted which includes distortion and noise in current waveform, illusionary reactive power, and parasitic capacitance. Therefore, this scenario is performed to observe whether replacing the HUT with a normal load bank (resistor) poses some challenges or not. As the load bank is SP resistor, as simple model is developed in Simulink with a SP Thevenin equivalent of same parameters as that of MONA-8002. It's just an addition of current-controlled source to the model schematic shown in **Figure 5.9**, as now the measured current of the HUT needs to be fed back into the virtual model. A high value impedance is connected in parallel with the CC source block as in Simulink the CC source cannot operate in series with an inductive element. The schematic of the complete PHIL is shown in the **Figure 5.20** below.

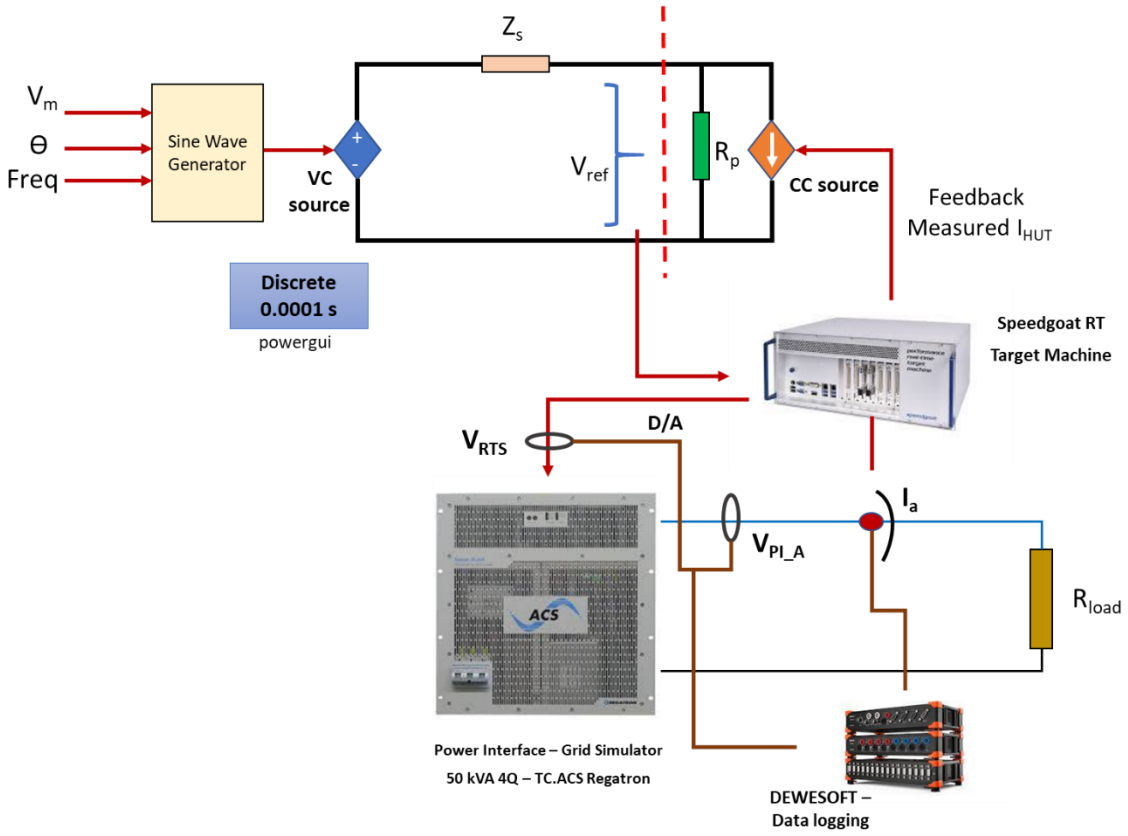


Figure 5.20 PHIL schematic with a constant resistive load bank as HUT.

The results are illustrated in the **Figure 5.21** below. The value of 100 V_{rms} nominal voltage is selected due to the power limitations of the load bank and to prevent over heating of the resistor.

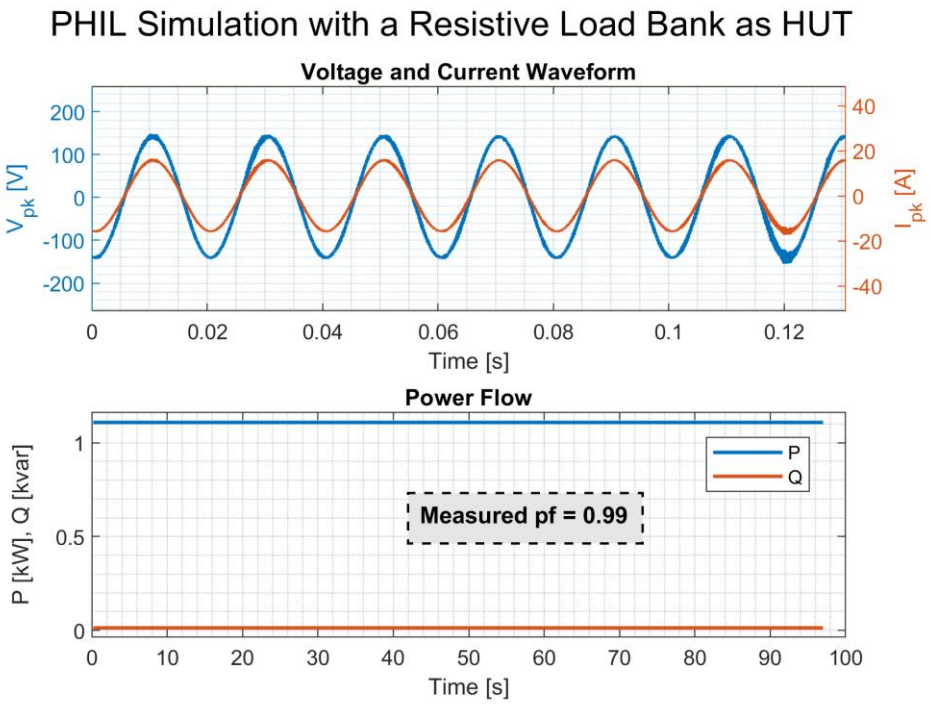


Figure 5.21 Results with HUT as a resistive load bank.

As expected, the HUT draws only active power and the pf of around 0.999 is measured. There is small inductance in the load of around 60 µH which renders a very negligible reactive power of around 0.02 kvar. Nevertheless, there is no unwanted illusionary powers in the system and also the smoothness of the current waveform is apparent from the first sub-plot. At some instants, the noise is captured at signal peaks but compared to the previous scenario the quality of the waveform has improved a lot. The voltage and current are completely in phase with each other. The result looks much similar to the one observed in case of a complete offline hybrid simulation with a resistive load in **Figure 4.4.** The quality of the signals could be improved further if the model is simulated with a lower sample-time. However, it was not possible due to the limitation of the processors.

Based on the results from this scenario, it can be established that the current-controlled amplifier as a HUT is solely responsible for introducing unwanted reactive power. The current waveform also becomes distorted with noise which ultimately leads to harmonics in the system and affects the real-time measurements.

5.5 Scenario – 4. Methods to Improve HUT Performance

To control the export of capacitive reactive power from the HUT, two simple yet effective measures are implemented as explained in this scenario.

5.5.1 Static Compensation

The first approach is the static compensation for the reference current signals. There is a phase difference between the voltage and current, by static compensation the idea is to mitigate this phase difference. Although for a resistive load, the I_{ref} signals generated in virtual simulation are in phase with the voltage but in reality, there is a shift due to the HUT capacitance as observed in scenario 2 in

section 5.3 . So, via this compensation method after the I_{ref} is generated a delay will be introduced in the simulation platform before sending the signal to the RT simulator. This time delay will be equivalent to the phase difference observed between the voltage and current for a particular power demand in usual case of no compensation. All the three phase currents will be subjected to an intentional delay in time domain. The following block diagram explains the compensation method to be implemented.

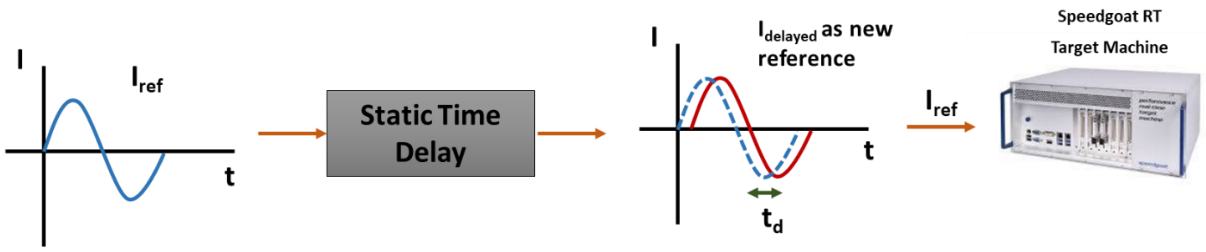


Figure 5.22 Static compensation for reference current signals of the HUT (CC Amplifier).

The I_{ref} calculated based on the power set-points and phase voltage at the interface bus is now subjected to a delay in time domain. To set the static time delay, the phase difference between V and I is required when the HUT is operating without any compensation. The phase difference of almost 20° is observed in a usual case, for an active power demand of 3 kW. Thus, an equivalent time delay will be evaluated, and all the three phase currents will be delayed by this particular time. The time delay can be calculated as shown in the following **Equation(21).**

1 Grid period -> 20 ms = 360°, so for 20°:

$$360° = 20\ ms \rightarrow 20° = \frac{20\ ms}{360°} * 20° = 1.11\ ms \tag{21}$$

For instance, phase A (I_{ref}) starts from 20° instead of 0° after implementing the static compensation. Thus, instead of resistive currents a lagging current waveform will be sent as a reference to compensate for the capacitance. However, the static compensation comes with certain limitations, the time delay calculated above is for the case when the power set -point is at [3 kW, 0 kvar] i.e. a pure resistive load. For each power set-points, first the need would be to run the usual case without compensation, observe the phase difference and then introduce the equivalent time delay. The information from the usual case scenario is necessary to implement the static compensation. To overcome this, another method is tested as explained below. The results of both the compensation methods are then discussed for comparison.

5.5.2 Dynamic Compensation

In this approach, the time delay to be introduced is calculated dynamically in the simulation platform. As the measured I_{HUT} is sent back to the virtually simulated model, the Fourier Transform of the signal is performed at the fundamental frequency to observe its phase angles. The harmonic components of the feedback current are not considered while compensation. The phase angles of measured I_{HUT} are compared with the generated I_{ref} to calculate the phase difference and ultimately the equivalent time delay. All this happens during the execution of the model in real-time. To shift the signal in time domain, Variable Time Delay block of Simulink is used in both the compensation methods. The following **Figure 5.23** illustrates the idea for the dynamic compensation method.

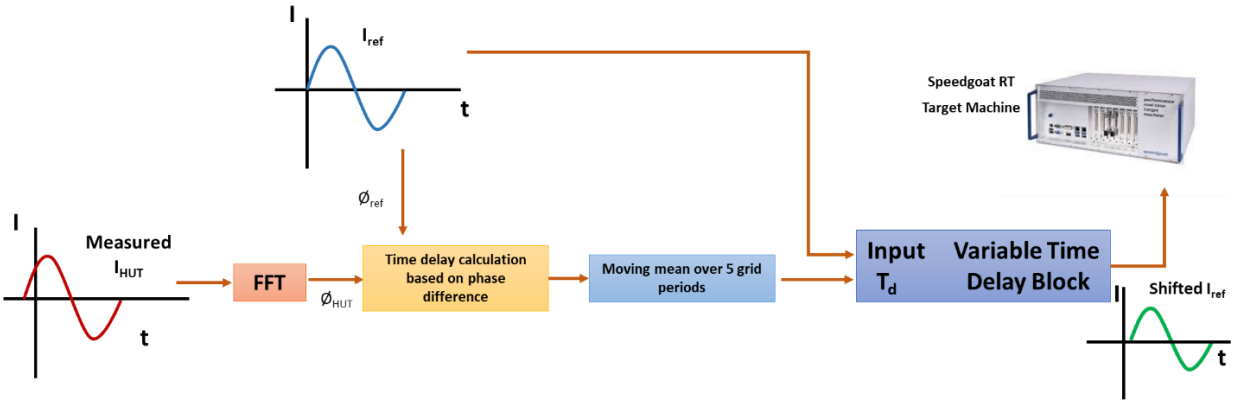


Figure 5.23 Dynamic compensation for reference current signals of the HUT (CC Amplifier).

As seen in the **Figure 5.23** above, the time delay is evaluated dynamically based on the comparison with the reference current signal. So, for stability, the moving mean of time-delay is evaluated over a period of 100 ms before shifting the signal in time-domain. Initially, the simulation will be executed normally without any compensation for one complete cycle of 20 ms, to have the feedback current as a base for comparison with the reference. Afterwards, the compensated signal is transmitted as a new reference. The moving average block from Simulink is used to calculate the moving mean over time.

The time delay compensation techniques implemented will not affect the dynamic behavior of the simulated model. Through these methods, the power angle (i.e. the power factor) of the physical power system is corrected to get closer to an ideal simulation scenario, so the illusionary powers could be controlled. The PHIL simulation results are shown below with and without compensation methods.

Parameters set in this case are:

V_{nom} = 400/sqrt (3) V_{rms}; Sample Time = 100 µs; Z_s= [0.0218 Ω, 68 µH]; P_{ref}= 3 kW, Q_{ref}=0 kvar; HUT operating as current-controlled amplifier.

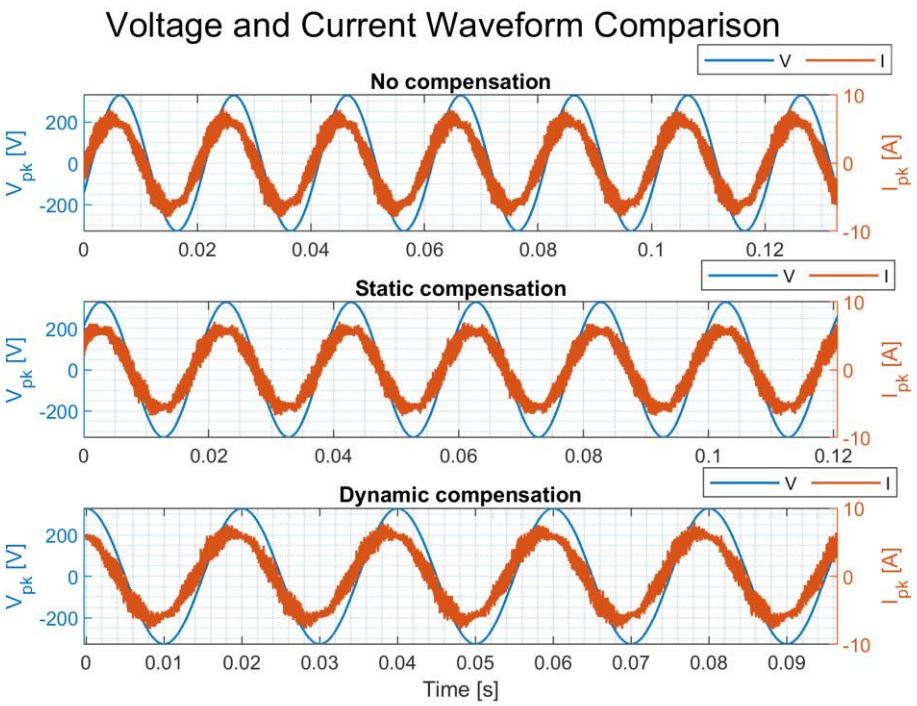


Figure 5.24 Measured V and I waveforms with and without I_{ref} compensation.

The first subplot shows the waveforms without any sort of compensation. Only active power [3 kW] is desired but it is obvious that the V and I are not exactly in phase. Also, the current waveform is very noisy as it incorporates all the harmonics additional to the fundamental component. The second and third subplots are with static and dynamic compensation of I_{ref}. The improvement is visible with static compensation with the current waveform a bit shifted to align with the voltage. For dynamic compensation, the result is not as good as static compensation and the improvement is hard to visualize. For better visualization, the power flow for all the cases is plotted as shown in the **Figure 5.25** below.

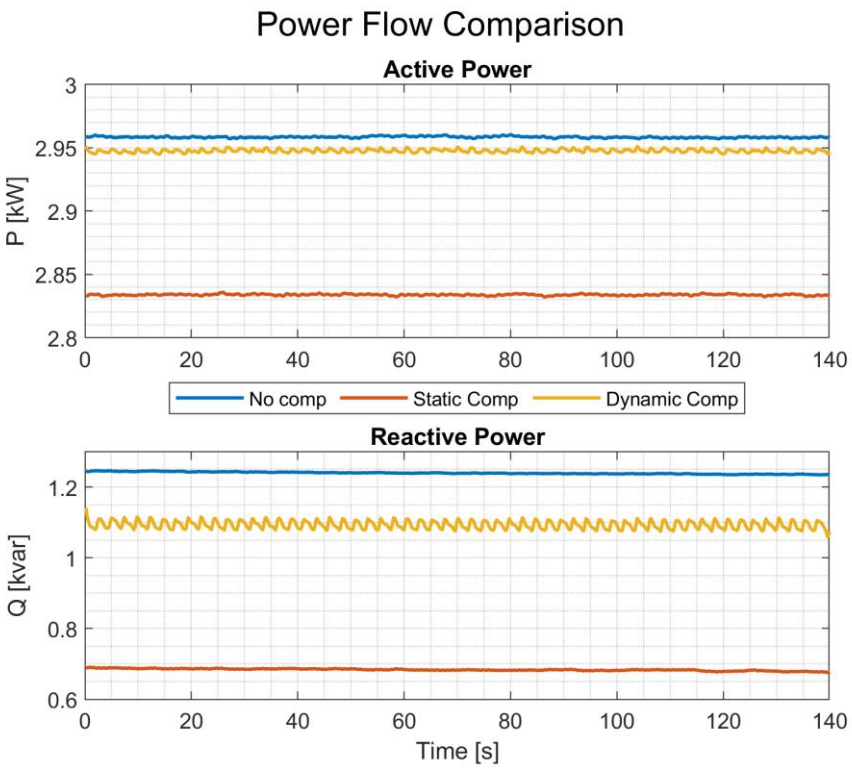


Figure 5.25 Measured power flow of the simulated PHIL system with and without compensation.

The first sub-plot represents active power flow and for all the cases it is closed to the commanded active power i.e. 3 kW. In case of static compensation (red line), the consumption is a bit less around 0.1 kW as compared to actual case, but the difference is not significant. The second sub-plot represents the capacitive reactive power from the HUT and interestingly the results have improved with compensation. The static compensation shows a significant decrease in reactive power fed to the source and has decreased by 0.5 kvar whereas in dynamic compensation (yellow line) it has decreased by 0.15 kvar. The overall performance has improved, and the HUT now injects less reactive power into the network compared to the usual case with around 1.25 kvar. The power profile for dynamic compensation are oscillatory. This is due to the fact that in this method the phase difference between V and I is calculated during RT simulation and due to the noise of the feedback current the phase difference is not constant. This introduces the oscillations, as dynamic compensation tries to catch up with the fluctuating difference and tries to minimize it. The static compensation on the other hand reduces the default reactive power significantly while maintaining to consume approximately the same active power as commanded.

With different active power loading of the HUT, the phase difference between the voltage and current gets better i.e. the power factor is improved. This can be observed from **Figure 5.16** in **section 5.3**, when the commanded active power was 5.34 kW, the current waveform is very smooth with a minor phase difference. On the contrary, in **Figure 5.24**, for a usual no compensation case with power setpoint of 3 kW the current waveform is very distorted and the phase difference is also higher.

5.5.3 Impact of Increasing Power Demand on the Power Factor.

To investigate the relation of HUT loading with the power factor of the system an experiment is conducted. The same MONA-8002 is simulated in real-time, and the active power demand is changed dynamically during the RT simulation. The reactive power setpoint is set to zero as usual. The model is

executed at first without any current compensation method. The same is then implemented with static and dynamic compensation to observe how much the compensation contributes towards the improvement of power factor compared to the usual case. At each power demand the phase difference would be different. So, for static compensation, the required static time delay based on the phase difference at each power demand is computed from the results of the first usual case. The results obtained are illustrated below:

Parameters set in this case are:

V_{nom} = 400/sqrt (3) V_{rms}; Sample Time = 100 µs; Z_s= [0.0218 Ω, 68 µH]; P_{ref} → [1 kW to 8 kW], Q_{ref}=0 kvar; HUT operating as current-controlled amplifier.

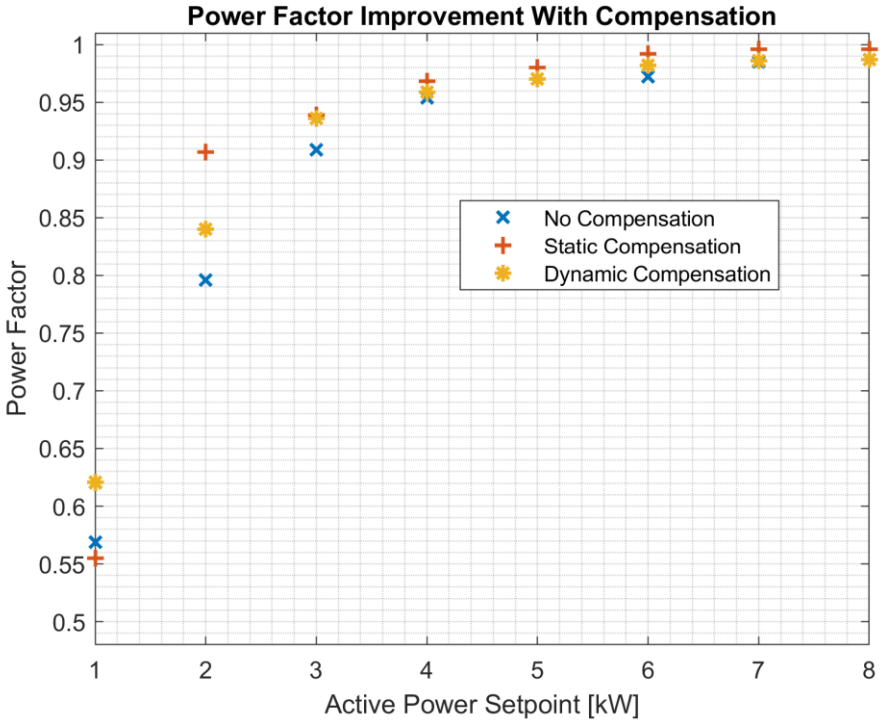


Figure 5.26 Impact of increased power loading on pf of the system with and without compensation.

The load is operated at nominal voltage at which the default reactive power is around 1.27 kvar , which meas that with the increasing active power demand the pf will also improve to keep the default reactive power same. This can be understood by **Equation (9)**, but to completely reduce the default reactive power the pf should be 1. The compensation is impelented to achieve the same. In **Figure 5.26** above, it can be observed that when the power demand is very low upto 2 kW, the pf of the system is very worse within the range of 0.8.

However, with current compensation the improvement of the pf is apparent. At low power demand, the static and dynamic compensation shows a signifiicant improvement although the pf is still not 1 but much better than the usual case. For instance, at 2 kW with static compensation the pf reaches to 0.9 which in usual case is 0.8. Similarly, the dynamic compensation also shows almost the same improvement in pf as of static compensation between the power demand range of 3 – 8 kW. Additionally, at lower power demands the pf is also very low. This shows that the quality of the current waveform would be very distorted with noise and harmonics. At a high power demand, from 6 kW onwards even the usual case has a good pf whereas the compensation adds further a little

improvement to take it more close to 1. It should be kept in consideration that at high active power even if the pf is 0.99 , there will be a significant reactive power. This is the reason, that at higher demand although the pf improves alot but the default reactive power is still present.

The improvement of pf with current compensation contributes towards the reduction of default reactive power. To visualize the difference, the reactive power is measured for each power demand under each case with and without compensation. The average reactive power for each case is plotted to obtain the following bar graph shown in **Figure 5.27.** As the power demand is increased dynamically in this scenario and the difference between each setpoint is around 1 kW , the current waveform gets very distorted and the HUT takes some time to achieve stability when the power demand is increased suddenly. The values of reactive power at each setpoint are considered after the HUT reaches some stability and the current waveform is smooth otherwise the dominant harmonics would affect the observations.

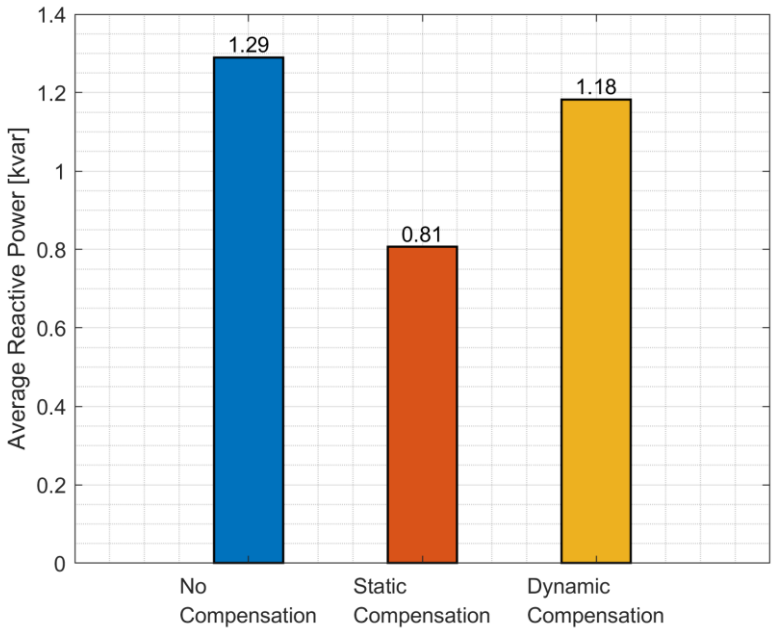


Figure 5.27 Average reactive power flow from the HUT towards the source with and without compensation.

On average, at a standard phase voltage the capacitive reactive power from the HUT is around 1.29 kvar. With dynamic compensation this value is reduced to 1.18 kvar and the best case is with static compensation with a reduction of approximatey 0.5 kvar. Thus, the reactive power is not eliminated completely but improved with the current compensation. In a usual case, for HUT there will be a reactive power of 1.29 kvar which needs to be taken into account. The Regatron amplifiers have a bandwidth of 5 kHz and the Dewesoft device logging the data has the ability of capture the values upto 40 kHz. These values of reactive power are inclusive of all the harmonics present due to the noise and distortion of the signals at low power demands. If only the values at the fundamental frequency component is observed the default reactive power would be much less after compensation. However, the values with harmonics are opted to present a more realistic overview.

5.6 Summary

The results shows that the HUT in current-controlled amplifier mode introduces significant distortion in current waveform. The harmonics are very significant if the commanded power is very low between

the range of 0 – 3.5 kW. With this performance of the HUT, it would not be very useful to integrate dynamic household load profiles for the PHIL setup as the power demand of a household is in the same range. The presence of reactive power is still siginificant even after the compensation which makes it complicated to test the Q-management and bi-directional power flow from the HUT. The accurate observation of voltage regulation due to controlled feed-in from the HUT cannot be analyzed in this condition.

Further, the network is modelled with a sample time of 100 µs which is apparently not the best approach as it deteriorates the quality of the signal generated by the real-time simulator. Lower sample times are not possible as the processors are unable to handle signal generation and the system gets overloaded. Infact, MONA-8008 was also not possible to be executed in real-time on target due to the CPU overload. The use of FPGA's for signal generation blocks of the model would be an alternative as it would allow to build the model with lower fixed discrete sample times of 5 - 10 µs. This will impact greatly on the quality of the signals being generated in real-time.

6 Conclusion and Future Work

6.1 Outlook

In the first part of the thesis, the distribution grid model is developed in the phasor framework. The dynamic power flow analysis of the grid is conducted. The model serves as a convenient base to study the inverter-based generation impacts at LVDG level. It is executed with a fixed sample time of 100 ms and captures the voltage variations at the fundamental frequency due to power feed-in. The response of smart inverter block is also tested by implementing different state-of-the-art Q-management functions for the inverter including the voltage dependent reactive power injection.

The results of the complete phasor simulation depict the effectiveness of the hybrid load block as a source and sink. The simulation environment is quite useful for studying the voltage stability analysis without going into the detailed model of PV unit unless power quality and inverter harmonics analysis is the main focus. The grid following inverter model works efficiently as a simple P-Q source and allows to couple the Q-management functions as a top control layer. The reactive power injection from the inverter is limited according to the VDE guidelines to resemble the behavior of commercial inverters being deployed at distribution grid levels. The constant power factor, cosφ (P) and volt-var capability is explored for the grid voltage stability.

The process for developing the hybrid simulation model is established with suitable variable interchange between the two sub-systems (Phasor and discrete domain). The results of the hybrid simulation model show that the transfer of boundary variables between the two sub-systems is accurate including the exchange of active and reactive power at the interface bus. The sub-systems are represented using the Thevenin and Norton equivalents, respectively. The voltage and current values are compared at the interface bus from both the domains. Consequently, the power transfer is also validated successfully once with a conventional load in discrete domain and once with a hybrid load.

The hybrid simulation approach saves the need for developing the whole grid model in discrete domain for PHIL simulation. Only the partition at the PCC is performed so that during the PHIL simulation the voltages at the PCC are sent as reference to the RT simulator for the power interface. Furthermore, it also provides the interface to deal with measured feedback currents during PHIL, as the current of HUT can be integrated as a source signal for the current sources modelled in the simulation environment. Basically, it resembles the PHIL ITM voltage type interface which also uses the Thevenin equivalent circuit to represent the distribution grid model. For future work, the developed hybrid interface can also be used to study the switching impacts of inverter-based generation by having a detailed inverter model in discrete domain.

Within the scope of the PHIL, the dynamic behavior of the physical power components is studied. The open circuit test is performed to analyze the voltage offset pertaining to the PI. The characteristic of the PI is established to evaluate its offset at respective voltage levels. The phase difference between the reference voltage and the amplified output voltage is also highlighted. For the close-loop PHIL, different hardware configurations are tested as load. Firstly, the amplifier is operated in RLC load simulation mode and it has been discovered that despite the configuration being set to a pure resistive load, a capacitive reactive power is present. The same phenomenon is observed when the amplifier is operated in current-controlled mode. The reference current evaluation model is developed virtually

which generates reference current signals for the HUT in CC amplifier mode. The intention to draw only active power is not fulfilled due to the parasitic capacitance of the HUT.

At standard voltage level, the reactive power of roughly 1.27 - 1.3 kvar is fed into the grid by the HUT. When the HUT is replaced with a resistive load bank, no such phenomenon is observed and only the desired power is being consumed from the grid side. The compensation methods are developed to mitigate the default reactive power by introducing a calculated time delay in the reference current signal equivalent to the phase difference between the voltage and current in usual case. Although, the compensation methods do not mitigate the reactive powers completely but are found to be effective to a certain extent. The static compensation drops down the reactive power by 0.5 kvar while the dynamic compensation is not as efficient as the static one but stills contributes towards reducing the default reactive power by 0.1 kvar on average.

The first up challenge related to the PHIL simulation is the sample-time. The model is executed on multi-core processors in real-time which poses a computational limitation. The lowest limit of 100 µs is achieved which apparently effects the quality of the reference voltage and current signals. Alternatively, the model blocks containing the discrete signal generation can be shifted to FPGA which enables enhanced performance compared to the processors. The processors have limitations and an attempt to execute the model with lower sample-times prompted CPU overload. Secondly, the CC amplifier causes harmonics leading to a deteriorated current waveform. At lower active power demands, the current waveform is found to be quite distorted and the power factor of the system is affected badly. Although the current waveform and the power factor gets better with high active power demands, the unwanted reactive power is still a problem. The data measuring device used has the ability to capture harmonics at higher frequencies and it is established that if only the fundamental frequency components are considered, the compensation method would turn out to be more effective reducing the default reactive power further more.

However, the harmonics cannot be avoided as it affects the measurements and cause deterioration of the current waveform. This would not only affect the stability of the PHIL but also contribute towards the increase in time delay of the whole setup from sending the reference voltage to receiving the current feedback. The whole idea is to control the HUT to have the desired power consumption or feed-in, especially to simulate the behavior of a low voltage grid prosumer. But the response of CC amplifier as HUT under the power range of [0-3.5 kW] is not very efficient and this is the average power demand of a normal household load as observed in phasor simulation. Additionally, testing the developed Q-management functions in PHIL would not be feasible in this condition as even after the compensation there is unwanted capacitive reactive power from the HUT.

6.2 Future Recommendations

PHIL simulations are complex, and its significance depends a lot on the dynamic behavior of the HUT. Specially in this case when the HUT is supposed to be controlled virtually from the model. The differences between the reference and generated signals should be compensated completely to permit validation of power control algorithms. The first recommendation as also discussed previously would be to make use of FPGA to have model sample-times of 5-10 µs or lower. Secondly, to develop a precise compensation algorithm using PID controller so that the difference can be tracked more accurately. Based on the results, it is recommended to compensate both the reference voltage and also the reference current before sending the respective signals to the PI and HUT.

Successful development of compensation algorithm would not only eliminate the effect of parasitic capacitance but also reduce the time delay of the whole PHIL setup. Furthermore, it is also necessary to compensate for harmonics as at low power demands the current harmonics are very dominant. For harmonics treatment the compensation of the signal can be performed in frequency domain. It would require phase-shifting of the signal harmonic-by-harmonic and phase-by-phase according to the time-delay, the approach is explained in [42] in which compensation is carried out for V_{ref}. The Fourier-transform of the signal is obtained and after introducing the phase-shift, the signal is reconstructed again in time domain before sending to the power interface. The stability study of the PHIL setup is not carried out in this thesis. After alleviating the differences, it is also recommended to perform the PHIL stability test with different HUT configurations. The Nyquist plot, Bode stability criteria, Routh criteria etc. are some of the stability evaluation methods for PHIL setup found in the literature.

7 References

[1] A. Marian, B. Bayer, H. Thomas, and P. Matschoss, “The German experience with integrating photovoltaic systems into the low-voltage grids: Introduction,” vol. 119, pp. 129–141, 2018. [Online]. Available: DOI.org/10.1016/j.renene.2017.11.045

[2] P. Matschoss, B. Bayer, H. Thomas, and A. Marian, “The German incentive regulation and its practical impact on the grid integration of renewable energy systems: Introduction,” vol. 134, 727-738, 2019. [Online]. Available: DOI.org/10.1016/j.renene.2018.10.103

[3] *Renewable Energy Sources Act - (Erneuerbare-Energien-Gesetz - EEG 2017). English translation reflecting changes formally adopted until July 2017: EEG*, 2017. Accessed: Mar. 24 2020. [Online]. Available: https://www.bmwi.de/Redaktion/EN/Downloads/renewable-energy-sources-act-2017.pdf

[4] *Generators connected to the low-voltage distribution network - Technical Requirements for the connections to and parallel operation with low-voltage distribution networks*, VDE-AR-N 4105, 2011.

[5] M. Kraiczy, L. Al Fakhri, T. Stetz, and M. Braun, “Do It Locally: Local Voltage Support by Distributed Generation –A Management Summary,” IEA Photovoltaic Power Systems Programme, 2017. Accessed: Mar. 19 2020. [Online]. Available: https://iea-pvps.org/wp-content/uploads/2020/01/Task_14_Report__Do_It_Locally_IEA_Final_T14.08.pdf

[6] The MathWorks, Inc., *MATLAB&Simulink*. Natick, Massachusetts, 2019. Accessed: Nov. 7 2020. [Online]. Available: https://ch.mathworks.com/downloads/

[7] T. Tjaden, J. Bergner, J. Weniger, and V. Quaschning, “Representative electrical load profiles of residential buildings in Germany with a temporal resolution of one second: Download,” HTW Berlin – University of Applied, Berlin, Germany, 2015. Accessed: Jul. 18 2020. [Online]. Available: DOI: 10.13140/RG.2.1.3713.1606/1

[8] Hochschule für Technik und Wirtschaft (HTW) Berlin, *PVprog-algorithmus: Download.* [Online]. Available: https://pvspeicher.htw-berlin.de/veroeffentlichungen/daten/pvprog/ (accessed: Aug. 9 2020).

[9] F. Plumier, “Co-simulation of Electromagnetic Transients and Phasor Models of Electric Power Systems,” Dissertation, Universitè de Liège, Liège, Belgium, 2015. Accessed: Dec. 7 2020. [Online]. Available: https://orbi.uliege.be/bitstream/2268/192910/1/thesis_cosim_FPlumier.pdf

[10] A. A. Van der Meer, M. Gibescu, M. A. M. M. Van der Meijden, W. L. Kling, and J. A. Ferreira, “Advance Hybrid Tranisient Stability and EMT Simulation for VSC-HVDC Systems,” vol. 30, no. 3, pp. 1057–1066, Dec. 2014. [Online]. Available: doi://10.1109/TPWRD.2014.2384499

[11] T. Yang, S. Bozhko, J. M. Le-Peuvedic, G. Asher, and C. I. Hill, “Dynamic Phasor Modeling of Multi-Generator Variable Frequency Electrical Power Systems: Abstract,” vol. 31, no. 1, pp. 563–571, 2016. [Online]. Available: DOI.org/10.1109/TPWRS.2015.2399371

[12] D. Athaide, “Electromagnetic Transient - Transient Stability Hybrid Simulation for Electric Power Systems with Converter Interfaced Generation,” Master’s dissertation, ARIZONA STATE UNIVERSITY, Tempe, Arizona, USA, 2018. Accessed: Nov. 7 2020. [Online]. Available: https://repository.asu.edu/attachments/211375/content/Athaide_asu_0010N_18449.pdf

[13] L. P. Piyasinghe, “Dynamic Phasor Based Analysis and Control in Renewable Energy Integration: REVIEW OF RELEVANT LITERATURE AND THEORY,” Dissertation, University of South Florida, Tampa, Florida, USA, 2015. Accessed: Nov. 7 2020. [Online]. Available: https://core.ac.uk/download/pdf/71955785.pdf

[14] A. Hariri, “Simulation Tools and Techniques for Analyzing the Impacts of Photovoltaic System Integration.: EMT Simulation,” Dissertation, Florida State University, Florida, USA, 2017. Accessed: Nov. 7 2020. [Online]. Available: http://purl.flvc.org/fsu/fd/FSU_2017SP_Hariri_fsu_0071E_13764

[15] A. Hariri and M. O. Faruque, “A Hybrid Simulation Tool for the Study of PV Integration Impacts on Distribution Networks,” vol. 8, no. 2, pp. 648–657, 2017. [Online]. Available: doi://10.1109/TSTE.2016.2614960

[16] T. H. DEMIRAY, “Simulation of Power Systems Dynamics using Dynamic Phasor Models: Introduction,” Dissertation, SWISS FEDERAL INSTITUTE OF TECHNOLOGY, Zurich, 2008. Accessed: Nov. 7 2020. [Online]. Available: doi://10.3929/ETHZ-A-005566449

[17] V. Jalili-Marandi, V. Dinavahi, K. Strunz, J. A. Martinez, and A. Ramirez, “Interfacing Techniques for Transient Stability and Electromagnetic Transient Programs IEEE Task Force on Interfacing Techniques for Simulation Tools,” vol. 24, no. 4, pp. 2385–2395, 2009. [Online]. Available: doi://10.1109/TPWRD.2008.2002889

[18] F. Plumier, P. Aristidou, C. Geuzaine, and T. Van Cutsem, “Co-Simulation of Electromagnetic Transients and Phasor Models: A Relaxation Approach,” vol. 31, no. 5, pp. 2360–2369, Mar. 2016. [Online]. Available: doi://10.1109/TPWRD.2016.2537927

[19] T. Fang, Y. Chengyan, W. Zhongxi, and Z. Xiaoxin, “Realization of Electromechanical Transient and Electromagnetic Transient Real Time Hybrid Simulation in Power System,” 2005. [Online]. Available: doi://10.1109/TDC.2005.1546932

[20] M. Zamroni, “Development of EMT / TS Co-simulation Using PowerFactory and PSS/E,” Master's Dissertation, Delft University of Technology, Delft, Netherlands, 2017. Accessed: Dec. 7 2020. [Online]. Available: http://resolver.tudelft.nl/uuid:644dd10c-b13d-4ed8-a15b-6927907cef10

[21] Hongtian Su, K. W. Chan, L. A. Snider, and J.-C. Soumagne, Eds., *Advancements on the Integration of Electromagnetic Transients Simulator and Transient Stability Simulator*, Jun. 2005.

[22] I. O. Akwukwaegbu and G. I. Okwe, “Concepts of Reactive Power Control and Voltage Stability Methods in Power System Network.: Reactive Power Control in Electrical Systems,” vol. 11, pp. 15–25, 2013. [Online]. Available: http://www.iosrjournals.org/iosr-jce/papers/Vol11-issue2/C01121525.pdf

[23] M. Braun et al, “Is the distribution grid ready to accept large-scale photovoltaic deployment? State of the art progress, and future prospects,” vol. 20, no. 6, pp. 681–697, 2011. [Online]. Available: DOI.org/10.1002/pip.1204

[24] S. Vlahinić, D. Franković, V. Komen, and A. Antonić, “Reactive Power Compensation with PV Inverters for System Loss Reduction,” vol. 12, no. 21, 2019. [Online]. Available: DOI.org/10.3390/en12214062

[25] S. Weckx and J. Driesen, “Optimal Local Reactive Power Control by PV Inverters,” vol. 7, no. 4, pp. 1624–1633, 2016. [Online]. Available: doi://10.1109/TSTE.2016.2572162

[26] T. Stetz, M. Rekinger, and I. Theologitis, “Transition from Uni-Directional to Bi-Directional Distribution Grids,” IEA Photovoltaic Power Systems Programme, Kassel, Germany, 2014. Accessed: Mar. 18 2020. [Online]. Available: https://iea-pvps.org/wp-content/uploads/2014/11/Transition_from_uni_directional_to_bi_directional_distribution_grids_REPORT_PVPS_T14_03_2014-1.pdf

[27] D. Fetzer, “Development of a MATLAB/Simulink Framework for Phasor-Based Power System Simulation and Component Modeling Based on State Machines,” Dissertation, University of Kassel, Kassel, Germany, 2018. Accessed: Jul. 13 2020. [Online]. Available: doi://10.19211/KUP9783737606097

[28] T. Stetz, “Autonomous Voltage Control Strategies in Distribution Grids with Photovoltaic Systems,” Ph.D. dissertation, Elect. Engg and Computer Science, University of Kassel, Kassel,Germany, 2013. Accessed: Mar. 9 2020. [Online]. Available: https://www.upress.uni-kassel.de/katalog/abstract_en.php?978-3-86219-712-5

[29] R. Brandl, “Operational Range of Several Interface Algorithms for Different Power Hardware-In-The-Loop Setups,” vol. 10, no. 12, Nov. 2017. [Online]. Available: DOI.org/10.3390/en10121946

[30] F. Lehfuß and G. F. Lauss, Eds., *Power Hardware-In-The-Loop Simulations For Distributed GENERATION*, 2011.

[31] C. Seitl, J. Kathan, G. Lauss, and F. Lehfu, Eds., *Power Hardware-in-the-Loop Implementation and Verification of a Real Time capable Battery Model*, 2014.

[32] RTDS Technologies, “Power Hardware in the Loop Simulation (PHIL),” RTDS Technologies 2-1, 2019. Accessed: Jul. 27 2020. [Online]. Available: https://knowledge.rtds.com/hc/en-us/articles/360037124014-PHIL-Report

[33] F. Ebe *et al.,* “Comparison of Power Hardware-in-the-Loop Approaches for the Testing of Smart Grid Controls,” vol. 11, no. 12, 2018. [Online]. Available: DOI.org/10.3390/en11123381

[34] REGATRON, “TC.ACS Full 4-Quadrant Grid Simulator; Device Manual.,” REGATRON, Rorschach, Switzerland Version V2.10, 2018. Accessed: Jul. 14 2020. [Online]. Available: https://www.regatron.com/service/download/manuals/tc.acs-series-manual.pdf

[35] L. Ibarra, A. Rosales, P. Ponce, A. Molina, and R. Ayyanar, “Overview of Real-Time Simulation as a Supporting Effort to Smart-Grid Attainment,” vol. 10, no. 6, 2017. [Online]. Available: DOI.org/10.3390/en10060817

[36] S. Spataru, J. Martins, D.-I. Stroe, and D. Sera, Eds., *Test Platform for Photovoltaic Systems with Integrated Battery Energy Storage Applications*: Institute of Electrical and Electronics Engineers (IEEE), 2018.

[37] Forschungsstelle für Energiewirtschaft e.V. - FfE, *Projekt MONA 2030 - FfE stellt rechenfähige Basisnetztopologien aus Projekt MONA 2030 zur Verfügung.* [Online]. Available: https://www.ffe.de/themen-und-methoden/speicher-und-netze/752-ffe-stellt-rechenfaehige-basisnetztopologien-aus-projekt-mona-2030-zur-verfuegung (accessed: Jul. 18 2020).

[38] Electric Power Research Institute, Inc, *OpenDSS-The Open Distribution System Simulator*. Palo Alto, California, 1997. Accessed: Aug. 9 2020. [Online]. Available: https://www.epri.com/pages/sa/opendss

[39] D. Pattabiraman, R. H. Lasseter., and T. M. Jahns, Eds., *Comparison of Grid Following and Grid Forming Control for a High Inverter Penetration Power System*: Institute of Electrical and Electronics Engineers (IEEE), 2018.

[40] *Voltage characteristics of electricity supplied by public distribution systems*, EN 50160.

[41] MathWorks, *Impedance Measurement - MathWorks Documentation.* [Online]. Available: https://ch.mathworks.com/help/physmod/sps/powersys/ref/impedancemeasurement.html (accessed: Jul. 25 2020).

[42] E. G. Sansano, A.J. Roscoe, and G.M. Burt, Eds., *Harmonic-by-Harmonic Time Delay Compensation Method for PHIL Simulation of Low Impedance Power Systems*: Institute of Electrical and Electronics Engineers (IEEE), 2015.

A. APPENDIX A – MONA Grid

A.1 Network Line Parameters.

Linecode	Resistance (Ω/km)		Reactance (mH/km)		Capacitance (nF / km)	
	Positive Sequence (r1)	Zero Sequence (r0)	Positive Sequence (l1)	Zero Sequence (l0)	Positive Sequence (c1)	Zero Sequence (c0)
NAYY 4x50	0.642	2.568	0.083	0.312	670	275.7
NAYY 4x120	0.255	1.02	0.08	0.292	797.3	365.9
NAYY 4x150	0.208	0.832	0.08	0.292	830	385.9
NAYY 4x185	0.167	0.668	0.08	0.292	868.2	409.3

A.2 MONA-8002 OpenDSS Script Power Flow Analysis with Feed-in Units.

```
Clear

set defaultbasefreq=50

New Circuit.MS Angle=0 Mvasc3=50000.0
basekv=10.0 bus1=M1 frequency=50 phases=3 pu=1.0 x1r1=1.66666666667

Redirect ..\linecodes.dss !linecodes containing line parameters
Redirect Monitors_8002_SP.txt !Monitors added to analyze voltage, current and power profiles at load buses

//---Trafo--//
New Transformer.8002 %Noloadloss=0.16825 Windings=2 XHL=3.91080554362 phases=3
~ wdg=1 conn=delta Bus=M1 kV=10.0 kVA=400.0 %R=0.42
~ wdg=2 conn=wye Bus=N1 kV=0.4 kVA=400.0 %R=0.42
//---

//----Lines---//
New Line.L0001 bus1=N1   bus2=S101 length=0.030 linecode=nayy4x185 phases=3
New Line.L0002 bus1=S101 bus2=S102 length=0.018 linecode=nayy4x185 phases=3
New Line.L0003 bus1=S101 bus2=H101 length=0.010 linecode=nayy4x50 phases=3
New Line.L0004 bus1=S102 bus2=H102 length=0.019 linecode=nayy4x50 phases=3
//-----

//---LoadShapes----//
New Loadshape.Shape_1 npts=86400 sInterval=1 mult=(file=Daily_1sprofiles_ONT_8002\H101P_a.txt)
QMult=(file=Daily_1sprofiles_ONT_8002\H101Q_a.txt) useactual=True
New Loadshape.Shape_2 npts=86400 sInterval=1 mult=(file=Daily_1sprofiles_ONT_8002\H101P_b.txt)
QMult=(file=Daily_1sprofiles_ONT_8002\H101Q_b.txt) useactual=True
New Loadshape.Shape_3 npts=86400 sInterval=1 mult=(file=Daily_1sprofiles_ONT_8002\H101P_c.txt)
QMult=(file=Daily_1sprofiles_ONT_8002\H101Q_c.txt) useactual=True
New Loadshape.Shape_4 npts=86400 sInterval=1 mult=(file=Daily_1sprofiles_ONT_8002\H102P_a.txt)
QMult=(file=Daily_1sprofiles_ONT_8002\H102Q_a.txt) useactual=True
New Loadshape.Shape_5 npts=86400 sInterval=1 mult=(file=Daily_1sprofiles_ONT_8002\H102P_b.txt)
QMult=(file=Daily_1sprofiles_ONT_8002\H102Q_b.txt) useactual=True
New Loadshape.Shape_6 npts=86400 sInterval=1 mult=(file=Daily_1sprofiles_ONT_8002\H102P_c.txt)
QMult=(file=Daily_1sprofiles_ONT_8002\H102Q_c.txt) useactual=True
```

```
New Loadshape.PV_1P npts=86400  sInterval=1  mult=(file=Daily_1sprofiles_ONT_8002\PV_H102.txt)
action=Normalize
//----

//---Loads----//
New Load.L101_1 bus1=H101.1 phases=1 kV=0.23094 yearly=Shape_1
New Load.L101_2 bus1=H101.2 phases=1 kV=0.23094 yearly=Shape_2
New Load.L101_3 bus1=H101.3 phases=1 kV=0.23094 yearly=Shape_3
New Load.L102_1 bus1=H102.1 phases=1 kV=0.23094 yearly=Shape_4
New Load.L102_2 bus1=H102.2 phases=1 kV=0.23094 yearly=Shape_5
New Load.L102_3 bus1=H102.3 phases=1 kV=0.23094 yearly=Shape_6
//-----

//-----Pv systems feeding at unity pf----//
New PVSystem.PV1 phases=1 bus1=H102.1 kV=0.23094
~ kVA=15 irradiance=1 Pmpp=15 yearly=PV_1P pf=1
New PVSystem.PV2 phases=1 bus1=H102.2 kV=0.23094
~ kVA=15 irradiance=1 Pmpp=15 yearly=PV_1P pf=1
New PVSystem.PV3 phases=1 bus1=H102.3 kV=0.23094
~ kVA=15 irradiance=1 Pmpp=15 yearly=PV_1P pf=1
//----

//---Set Iterations and solve----//
set Maxcontroliter=200
Set voltagebases=[10  .40]
Calcvoltagebases
solve

set mode=yearly number=86400 Loadshapeclass=yearly stepsize=1s  !One day simulation

Set overloadreport=true  ! TURN OVERLOAD REPORT ON
Set voltexcept=true     ! voltage exception report
set demand=true         ! demand interval ON
set DIVerbose=true      ! verbose mode is ON

Set Year=1
solve
closedi
```

B. Appendix B – Technical Datasheets

B.1 50 kVA 4-Q Power Amplifier (Power Interface)

The technical datasheets have been acquired from Regatron's official web resources.

TC.ACS.50.528.4WR.S.LC **50 kVA / 305 Vrms (L-N) / 72 A**

Technical Data

AC lineside ratings
Grid Port

Line voltage	3 x 360 – 528 V_{AC}
Line frequency	48 – 62 Hz
Mains connection type	3L + PE (no neutral)
Input current	3 x 360 V_{AC} / 90 Arms 3 x 400 V_{AC} / 81 Arms 3 x 440 V_{AC} / 74 Arms 3 x 480 V_{AC} / 68 Arms
Powerfactor (At nominal power)	1

Precharge unit provided. No inrush current.

AC loadside ratings
Simulation Port: 3L + N

Power range	0 - 50 kVA
Voltage range	0 – 305 Vrms (L-N)
Connection type	3L + N + PE
Current range	3 x 0 – 72 A[1)] 1 x 0 – 80 A[2)]
Frequency range	0 – 1000 Hz (see fig. 1,2)
Modulation bandwidth	5.0 kHz
DC offset	≤ 10 mV
Efficiency at nominal power	90 %

DC loadside ratings
Simulation Port: 3L + N

Configuration 1: two independent outputs
1 x 0 - 800 V_{DC}, ± 20 A, ± 16 kW (L1 - L2)
1 x 0 - 400 V_{DC}, ± 20 A, ± 8 kW (L3 - N)
Configuration 2: three independent outputs
3 x 0 - 400 V_{DC}, ± 20 A, ± 8 kW (L1 - N, L2 - N, L3 - N)
(total current in N is limited to 20A)

Static Accuracy

Voltage @ 50/60 Hz	0.05 % FS
Voltage general	< 1.5 V
Frequency	2 mHz
Phase Angle	1 °

Slew rate

Voltage slew rate	≤ 4 V / µs
10% … 90% step of full scale	≤ 100 µs (see fig. 4)

Harmonic distortion at 50 Hz (THD)[3)]

At linear loads	≤ 0.4 %
At non linear loads	≤ 1.6 %

DC ripple + noise

16Hz - 200kHz	230mV rms
9kHz - 20MHz	700mV p-p

Overloadability

up to 10 s every 600 s	≤ 150 % (see fig. 2,3)
up to 1 s every 60 s	≤ 200 % (see fig. 2,3)

Measurement Precision

Voltage	± 0.7 % FS
Current	± 1.4 % FS

1) Current according to the given power limit of the corresponding units
2) The 80 A 2-phase (or split-phase 120 VAC - Neutral - 120 VAC) can be supported with the following restrictions:
- No other phases under load
- Ambient temperature < 25°C
- The overloadability given on page 4 cannot be guaranteed.
3) Up to 290 Vrms (L-N)

Technical Data

Setpoint Resolution

Voltage	0.1 V
Frequency	1 mHz
Phase	0.1 °

Operating Modes

Full 4 quadrant Grid Simulation mode
Full 4 quadrant Load Simulation mode
Full 4 quadrant Amplifier mode CV / CC

Protection
Built-in Protection

Overvoltage protection	programmable
Overcurrent protection	programmable

Internal diagnostics
line input conditions, internal current conditions, temperature conditions, processor idle time, system configuration, system communication, sensor signals, power semiconductor temperatures, power conditions etc.
Type of Protection (according EN 60529)

Basic construction	IP 20
Mounted in cabinet	up to IP 54

Safety interface
The energy transmission between the line side and the load side will be disconnected via integrated safety relays. The interface provides a connection to an external safety circuit.

Conformity CE-Marking
EMC Directive

EMC emission	EN 61000-6-4
EMC immunity	EN 61000-6-2

Low Voltage Directive
Electronic equipment
for use in power installations EN 50178
RoHS Directive 2011/65/EU
Technical documentation for the assessment of electrical and electronic products with respect to the restriction of hazardous substances EN 50581

Ambient conditions
Operation

Operating temperature	5 – 40 °C
Relative air humidity (non-condensing)	0 – 95 %

Storage

Storage temperature	-18 – 70 °C
Relative air humidity (non-condensing)	0 – 95 %
Installation altitude	0 – 1000 m above sea level
Operating orientation	upside
Storage, transport orientation	upside

Utilization category

Protection class	I
Overvoltage category	III
Degree of pollution	2

Emission

Noise level	≤ 74 dB, at 1 m

Liquid Cooling (LC) Specifications
(aircooling possible with optional TC.LAE)

Material	Al
Inlet/outlet on rear side size	G ½"
Liquid temperature	15 – 50 °C
Range of flow rate	4 l / min (15°C) – 8 l / min (50°C)
Recommended flow rate	5 l/min
Operation pressure max.	4 bar
Pressure drop	70 mbar @ 5 l/min

B.2 30 kVA 4-Q Power Amplifier (HUT)

TC.ACS.30.528.4WR.S.LC — 30 kVA / 305 Vrms (L-N) / 43 A

Technical Data

AC lineside ratings
Grid Port

Line voltage	3 x 360 – 528 V_{AC}
Line frequency	48 – 62 Hz
Mains connection type	3L + PE (no neutral)
Input current	3 x 54 Arms
Powerfactor (At nominal power)	1

Precharge unit provided. No inrush current.

AC loadside ratings
Simulation Port: 3L + N

Power range	0 - 30 kVA
Voltage range	0 – 305 Vrms (L-N)
Connection type	3L + N + PE
Current range	3 x 0 – 43 A
Frequency range	0 – 1000 Hz (see fig. 1,2)
Modulation bandwidth	5.0 kHz
DC offset	≤ 10 mV
Efficiency at nominal power	90 %

DC loadside ratings
Simulation Port: 3L + N

Configuration 1: two independent outputs
1 x 0 - 800 V_{DC}, ± 20 A, ± 16 kW (L1 - L2)
1 x 0 - 400 V_{DC}, ± 20 A, ± 8 kW (L3 - N)
Configuration 2: three independent outputs
3 x 0 - 400 V_{DC}, ± 20 A, ± 8 kW (L1 - N, L2 - N, L3 - N)
(total current in N is limited to 20A)

Static Accuracy

Voltage @ 50/60 Hz	0.05 %
Voltage	< 1.5 V
Frequency	1 mHz
Phase Angle	1 °

Slew rate

Voltage slew rate	≤ 4 V / µs
10% ... 90% step of full scale	≤ 100 µs (see fig. 4)

Harmonic distortion at 50 Hz

Linear	≤ 0.1 %
Non linear	≤ 0.8 %

Overloadability

up to 10 s every 600 s	≤ 150 % (see fig. 2,3)
up to 1 s every 60 s	≤ 200 % (see fig. 2,3)

Measurement Precision

Voltage	± 0.7 %
Current	± 2.4 %

Setpoint Resolution

Voltage	0.1 V
Frequency	1 mHz
Phase	0.1 °

Operating Modes
Full 4 quadrant Grid Simulation mode
Full 4 quadrant Load Simulation mode
Full 4 quadrant Amplifier mode CV / CC

Technical Data

Protection
Built-in Protection

Overvoltage protection	programmable
Overcurrent protection	programmable

Internal diagnostics
line input conditions, internal current conditions, temperature conditions, processor idle time, system configuration, system communication, sensor signals, power semiconductor temperatures, power conditions etc.

Type of Protection (according EN 60529)

Basic construction	IP 20
Mounted in cabinet	up to IP 54

Safety interface
The energy transmission between the line side and the load side will be disconnected via integrated safety relays. The interface provides a connection to an external safety circuit.

Conformity CE-Marking
EMC Directive

EMC emission	EN 61000-6-4
EMC immunity	EN 61000-6-2

Low Voltage Directive
Electronic equipment
for use in power installations ... EN 50178

RoHS Directive 2011/65/EU
Technical documentation for the assessment of electrical and electronic products with respect to the restriction of hazardous substances ... EN 50581

Ambient conditions
Operation

Operating temperature	5 – 40 °C
Relative air humidity (non-condensing)	0 – 95 %

Storage

Storage temperature	-18 – 70 °C
Relative air humidity (non-condensing)	0 – 95 %

Installation altitude	0 – 1000 m above sea level
Operating orientation	upside
Storage, transport orientation	upside

Utilization category

Protection class	I
Overvoltage category	III
Degree of pollution	2

Liquid Cooling (LC)
Internal heat exchanger
(aircooling possible with optional TC.LAE)

Material	Al
Inlet/outlet on rear side size	G ½"
Liquid temperature	15 – 50 °C
Flow	4 l / min (15°C) – 8 l / min (50°C)
Pressure max.	8 bar

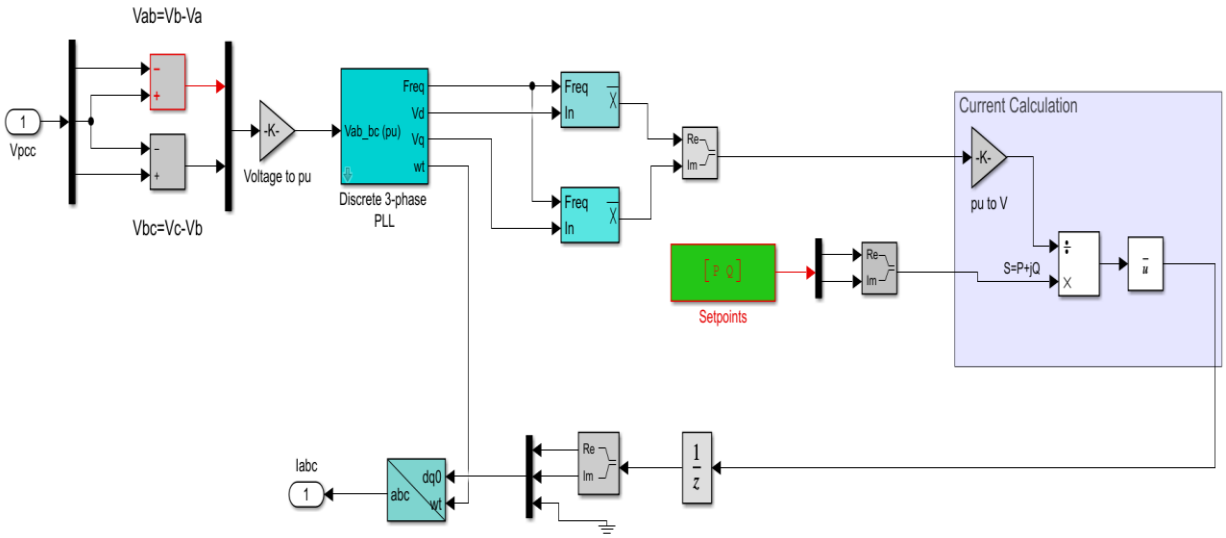
B.3 DEWESOFT – Analog Out Specifications

Analog out specification

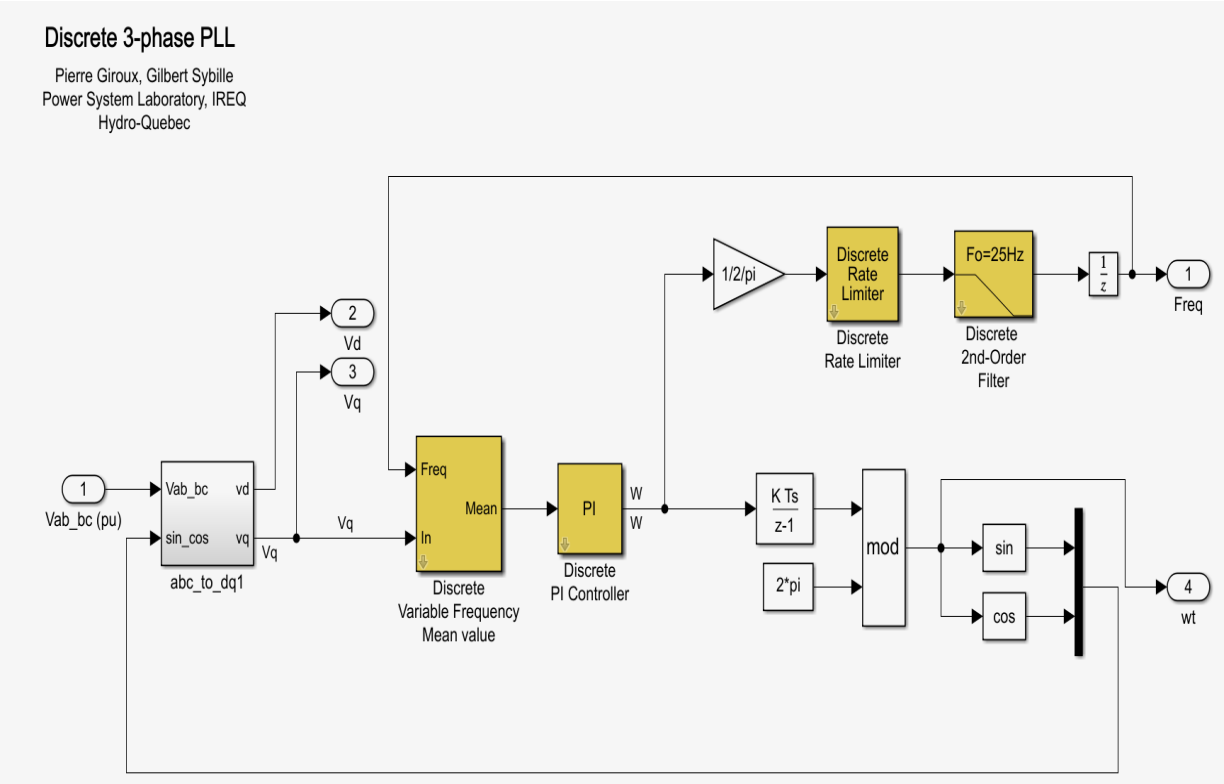
Outputs	**Voltage**		
DAC Type	24-bit delta-sigma		
Sampling Rate	Simultaneous 200 kS/sec		
Number Of Channels	8		
Function	File replay, conditioned AI output, FGEN (software option), channel output		
Specifications			
Full Scale	±10 V		
Analogue out bandwidth	40 kHz		
Accuracy	±0.1 % of reading ±0.02 V		
Temperature Drift	±50 ppm/K of reading ±200 µV/K		
Output configuration	Single Ended		
Typ. Noise floor @ 50 (200) kS/s output rate	-95 dB (-86 dB) @ 100 kHz Bandwidth		
Inter channel phase mismatch	0.1° * fout [kHz] + 0.1°		
THD	< -90 dB @ 1 kHz, 10 Vpeak-peak		
Output Impedance	< 1 Ω		
Maximum Output Current	20 mA		
Maximum load	> 1000 Ω		
Output Protection	Continuous short to ground		
Signal Delay	**100 S/s...50 kS/s**	**50 kS/s...100 kS/s**	**100 kS/s...200 kS/s**
Signal conditioning mode (see 1)	14 Samples + 50 µs	19 Samples + 2 µs	12 Samples + 35 µs
Additional Specifications			
Output connector	BNC		
1) SIRIUS-HD series does not support signal conditioning			

C. Appendix C – Simulink Model Blocks

C.1 Injection Current Evaluation Based on Power Setpoints



C.2 Discrete 3-Phase PLL Block



DECLARATION

I hereby confirm that this Master Thesis is entirely my own work. I confirm that no part of the document has been copied from either a book or any other source – including the internet – except where such sections are clearly referenced and the sources have been correctly identified in the list of references. Moreover, I confirm that I have taken notice of the 'Leitlinien guter wissenschaftlicher Praxis' of the University of Oldenburg.

Moiz

Oldenburg, 18th September 2020.